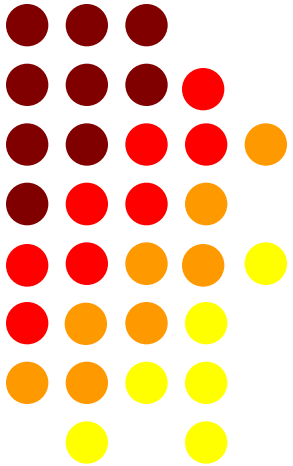
Lecture 15

Illustration of meaning of word transistor, its classification, introduction of structure of BJT, Explanation of current flow in BJT, Conditions for different regions of operation and their uses

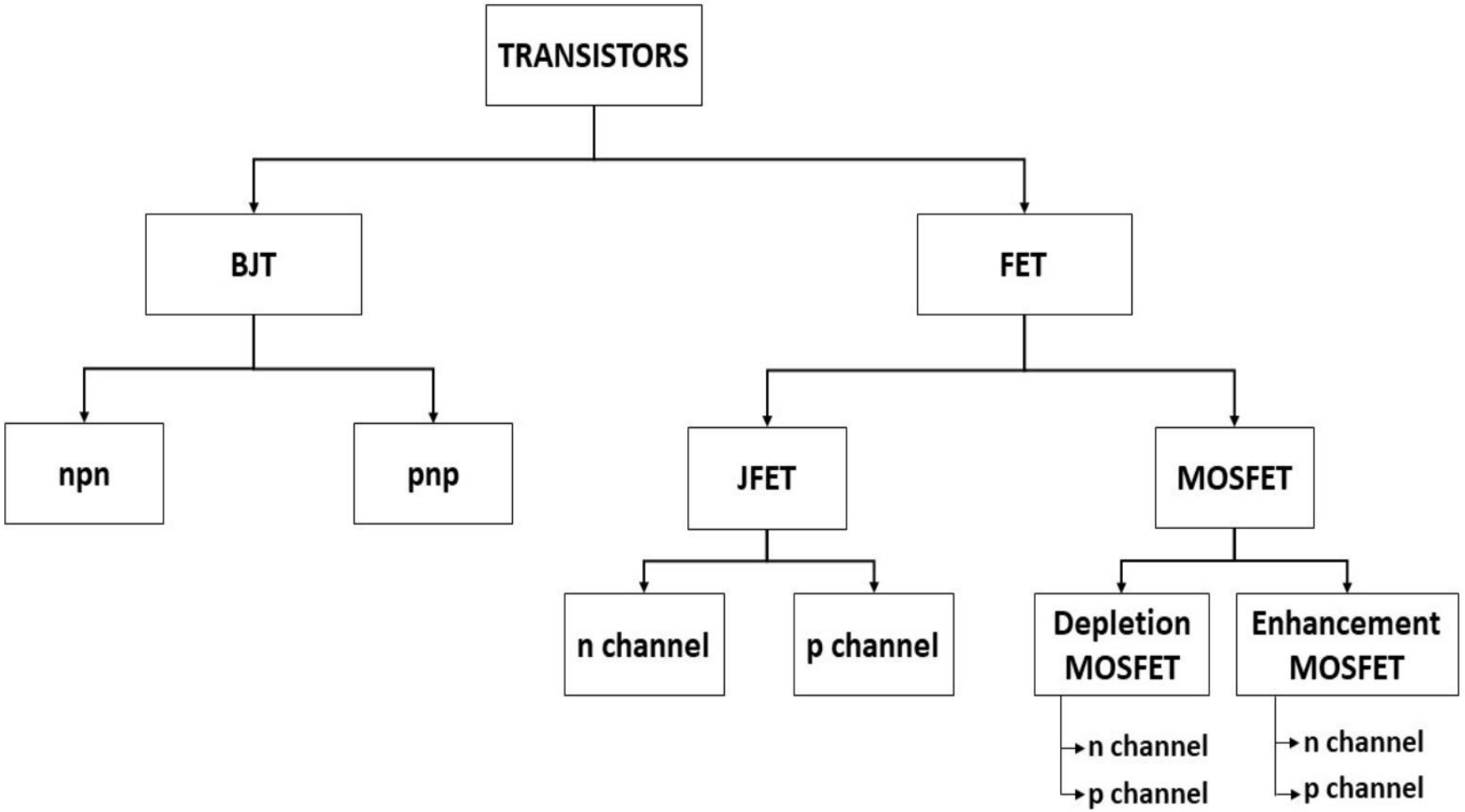


Transistor

- Transistor is a device which transfers applied signal from one type of resister to other type, For example signal can be transferred from low resistor to high or from high resistor to low resistor.

- “Transistor” (Transfer +resistor).
- Transistor is called bipolar device because its operation depends on the interaction of majority and minority carrier both.

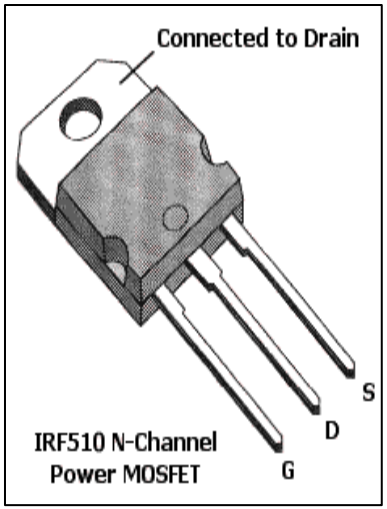
Classification of Transistor



FET: Field Effect Transistor

JFET: Junction Field Effect Transistor

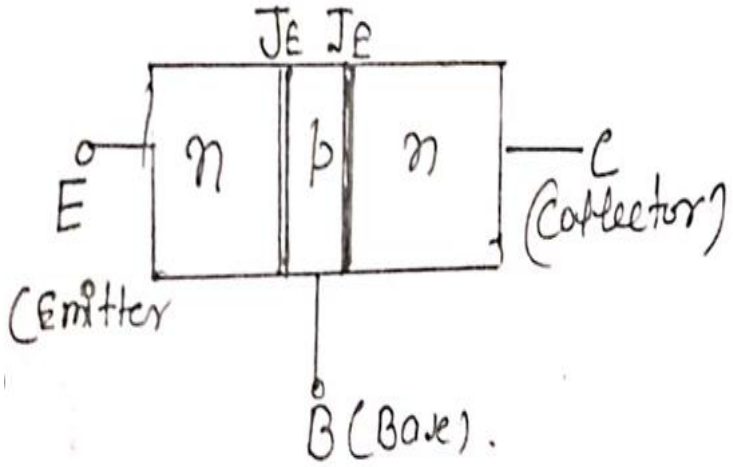
MOSFET: Metal Oxide Semiconductor Field Effect Transistor

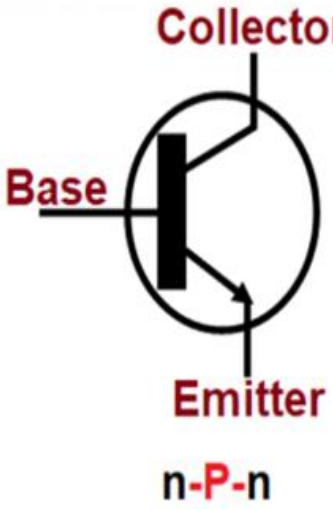


FET and BJT Transistor

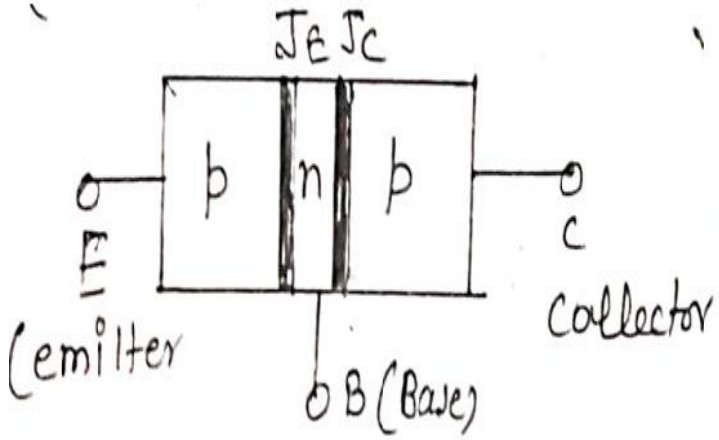
Construction of Transistor

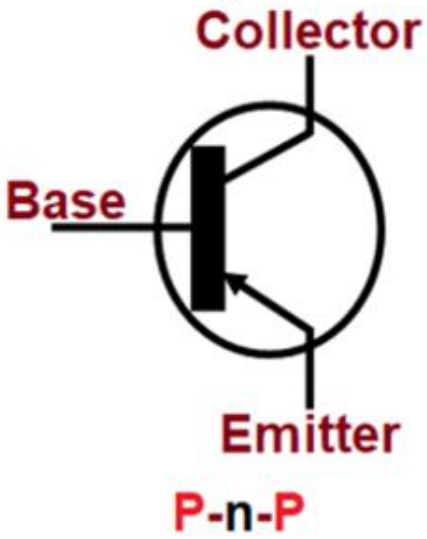
n-p-n





p-n-p





- **Emitter**: It is the highest doping region in the transistor. It supplies (emits) carrier to the base. It supplies electron to the base in n-p-n and holes in p-n-p.

- **Base:** The middle part of transistor is called base. It is very thin and lightly doped . So most of the carrier coming from emitter passes to collector.

- **Collector:** Collector collect the carriers which are coming from base. Doping of collector is heavier than base but less than emitter.

Area profile: C > E > B

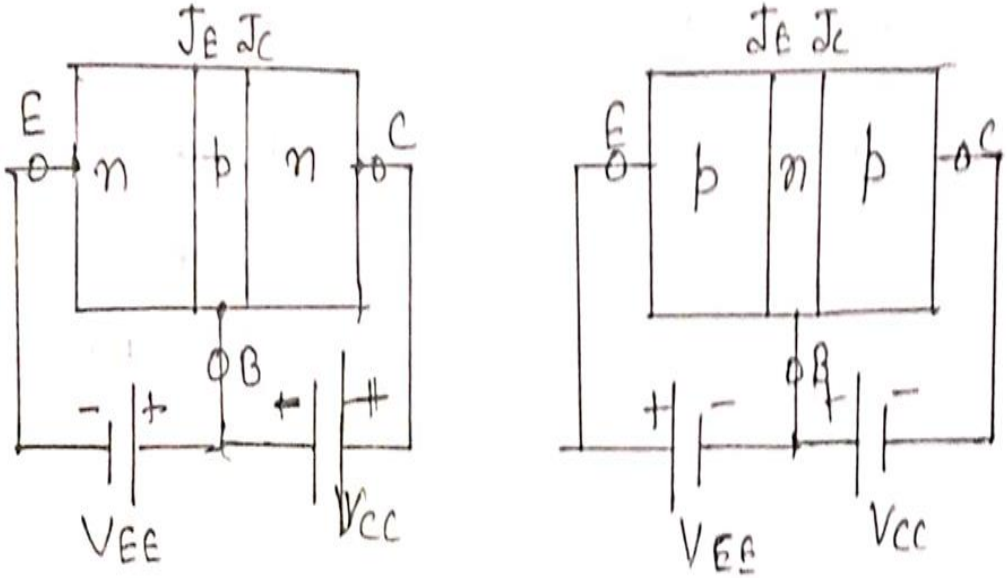
Doping profile: E > C > B

Mode or Working Regions of Transistor

- Transistor operates in three modes:

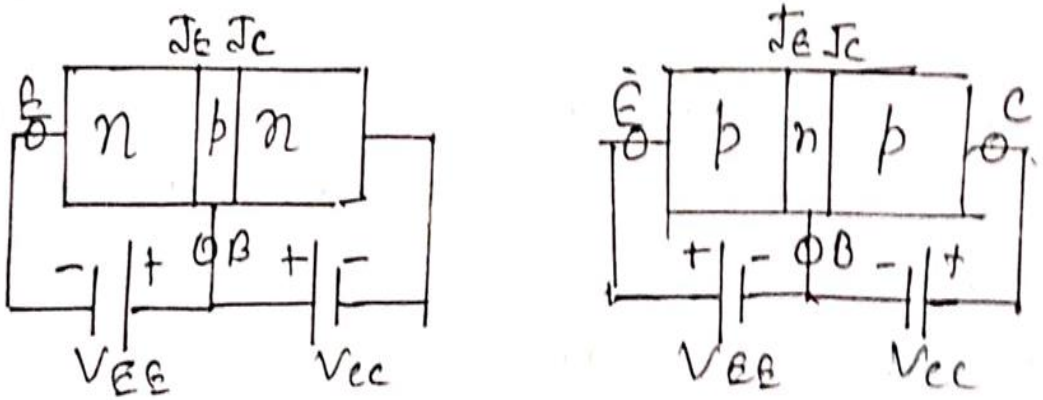
i) Active region:

- In active region emitter-base junction (J_E) is forward biased and collector -base junction (J_C) is reverse biased. In this region transistor works as an **amplifier.**



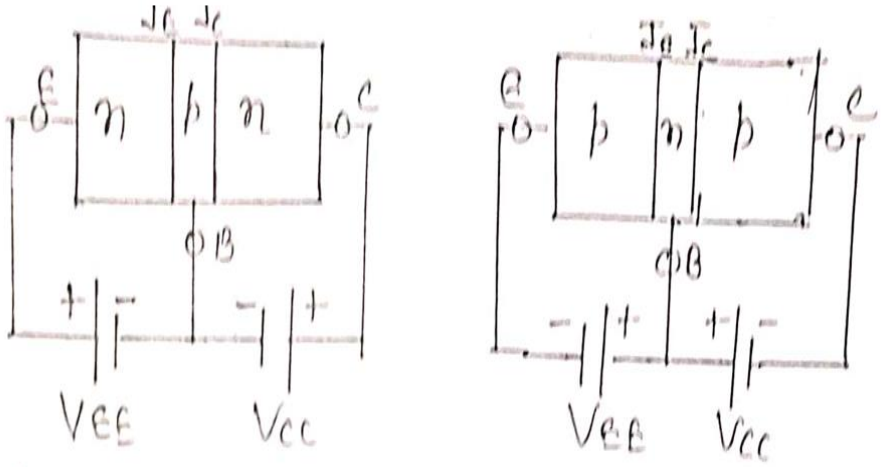
ii) Saturation region:

- In this region emitter-base junction (J_E) and collector -base junction (J_C) are forward biased. In this region transistor works as a **closed switch.**



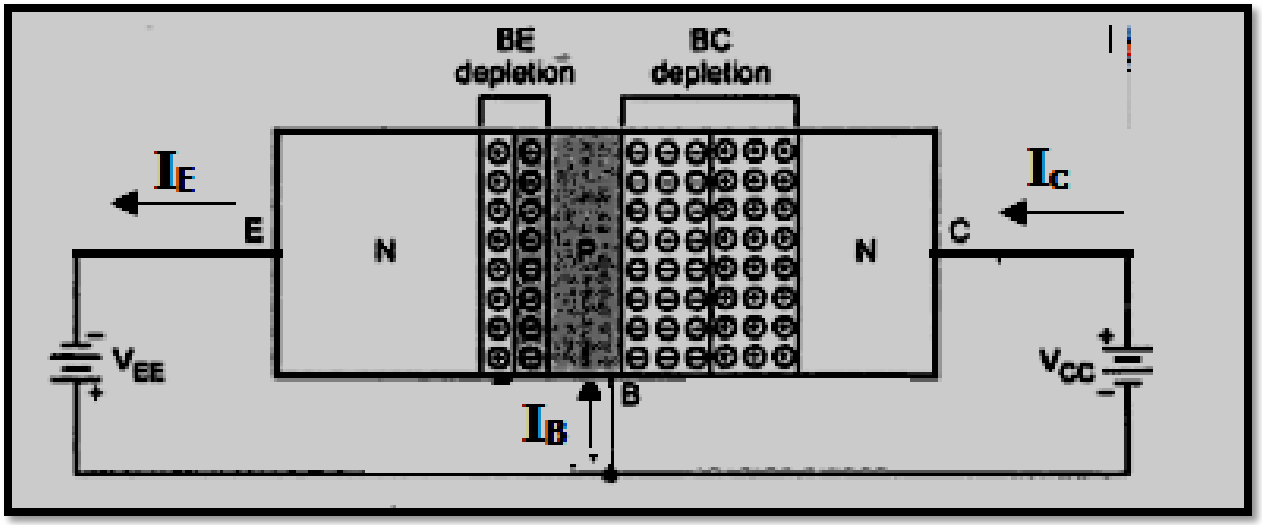
iii) Cut-off region:

- In this region emitter-base junction (J_E) and collector - base junction (J_C) are reverse biased. In this region transistor works as a **open switch.**



Operation of Transistor in Active Region

- To operate BJT in active region J_{EB} (emitter base junction) must be forward biased and J_{CB} (collector base junction) must be reverse biased.



Operation of Transistor in Active Region

- J_{EB} is forward biased by the battery V_{EE} by which the depletion region will decrease and a majority carrier flow will occur from emitter to base giving current $I_{majority}$ or I_E.

$$I_E = I_{majority} = I_{eE} + I_{hB}$$

- So, Here, I_{eE} is current due to electrons of emitter region and I_{hB} is current due to holes in base region.

Operation of Transistor in Active Region

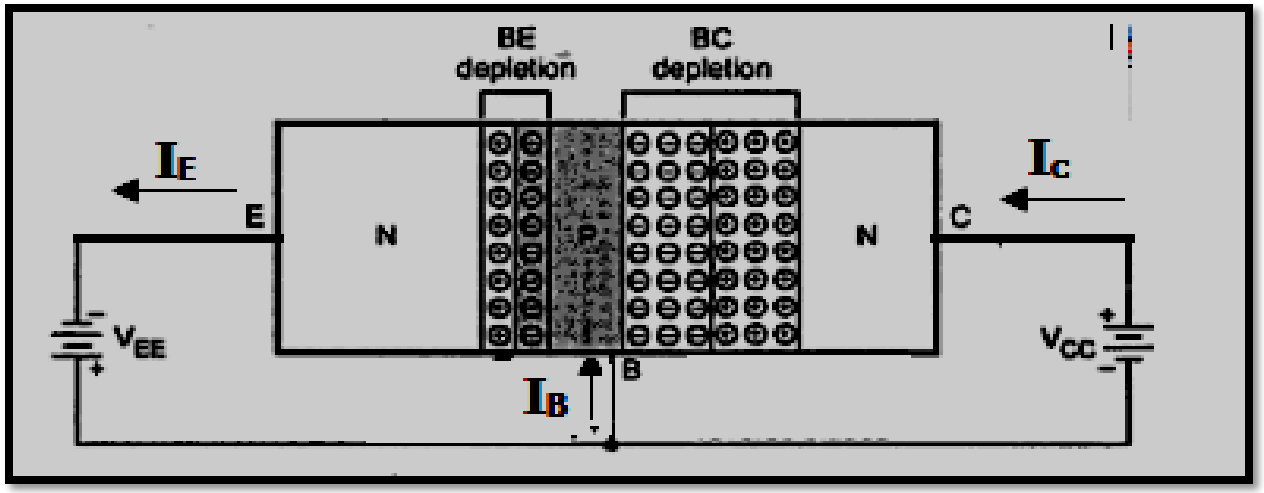
- In base region there is recombination between electrons and holes due to which base current is obtained. As number of holes in base is very small, base current is very small.
- J_{CB} is reverse biased by V_{CC}. So collector current is due to flow of minority charge carriers from both sides of the junction. In base minority carriers are electrons left after recombination and in collector minority carriers are holes. So,
- Directions of all terminal currents are shown in figure and it is clear that,

Operation of Transistor in Active Region

$$I_C = I_{minority} = I_{eB} + I_{hC} = \alpha I_E + I_o$$

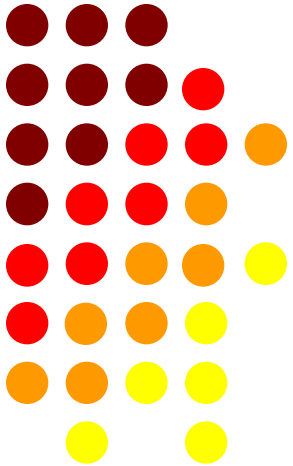
- Directions of all terminal currents are shown in figure and it is clear that,

$$I_E = I_C + I_B$$



Lecture 16

Introduction of CB Configurations of BJT: Structure, Current gain, Input Characteristics, Output Characteristics



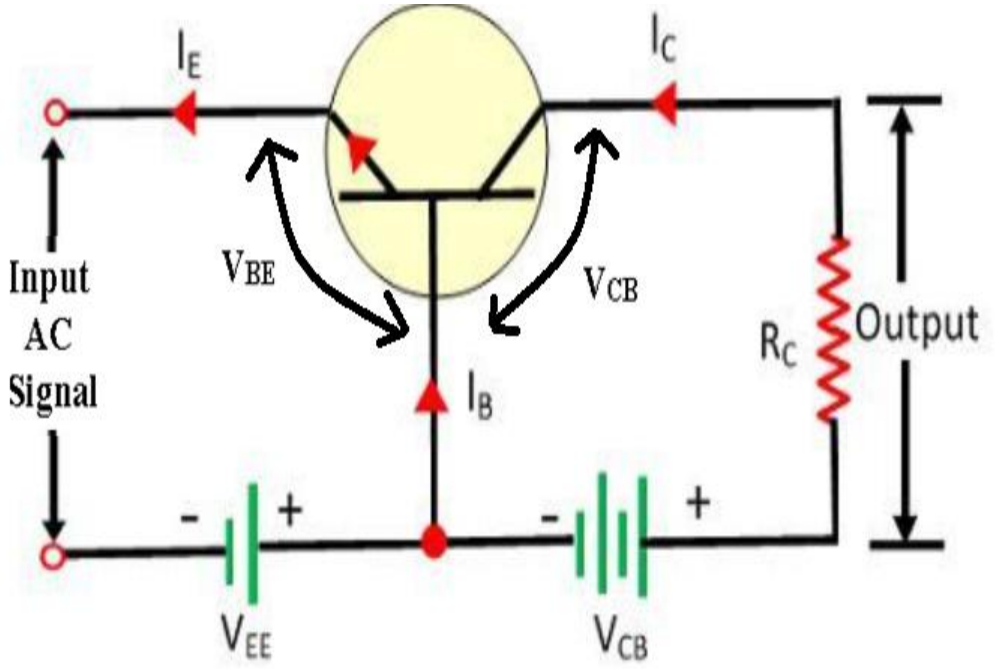
Transistor Configuration or Connection

- Transistor has three terminals emitter, base and collector. But we require four terminals to connect the transistor in a circuit as an amplifier. Two for input and two for output.
- This is achieved by making one terminal of transistor common to input and output.
- So, transistor has three configurations based on the common terminal.

i) Common base configuration (CB)
ii) Common emitter configuration (CE)
iii) Common collector configuration (CC)

Common base configuration (CB)

- Input is applied between emitter and base
- Output is taken out from collector and base
- Base is common between input and output.



i) DC Current gain:

- It is the ratio of output current (I_C) to the input current (I_E).

$$\alpha = \frac{I_C}{I_E}$$

- Since $I_E > I_C$ so value of α is less than 1
- Value of α ranges from .90 to .99
- So, no current gain is available in CB configuration.

Expression for Output Current

$$\mathbf{I_C = I_{C(Maj)} + I_{CO}}$$

For CB $I_{CO} = I_{CBO}$ (Collecter to base current when emitte

$$\mathbf{So\ I_C = I_{C(Maj)} + I_{CBO}} \ldots\ldots\ldots\ldots 1$$

$$\text{but } \alpha = \frac{I_{C(Maj)}}{I_E}$$

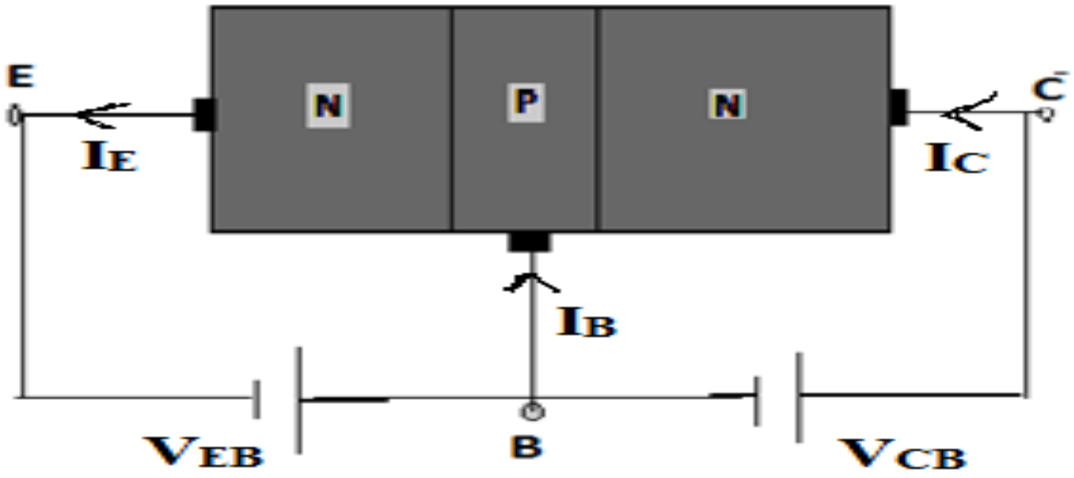
$$I_{C(Maj)} = \alpha I_E \ldots\ldots\ldots\ldots\ldots\ldots 2$$

Using 1 and 2

$$\boxed{\mathbf{I_C = \alpha I_E + I_{CBO}}}$$

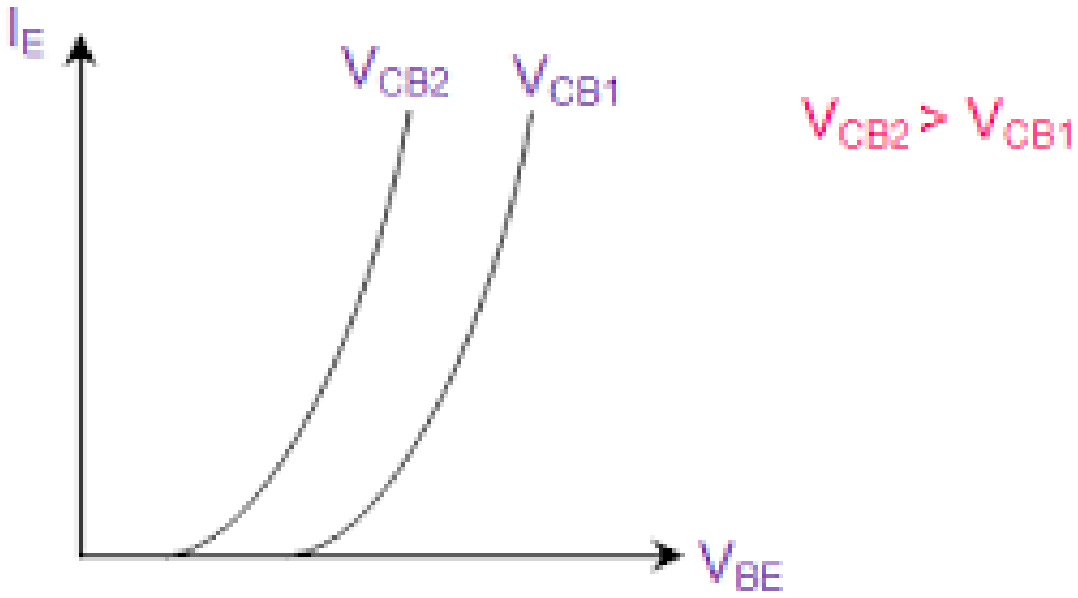
Input V/I Characteristics of CB Configuration

- It is graph between input current (I_E) and input voltage (V_{EB}) at constant output voltage (V_{CB}). This graph is drawn for active region of BJT.



Input V/I Characteristics of CB Configuration

- By keeping constant V_{CB}, when forward bias at emitter base junction is increased then graph between I_B and V_{EB} is similar to forward characteristics of pn junction diode. If this graph is again drawn for some higher value of V_{CB} a similar graph is obtained with reduced knee voltage.



Output V/I Characteristics of CB Configuration

- It is graph between output current I_C and output voltage V_{CE} at constant input current I_E. This graph is drawn for all three operating regions of BJT.

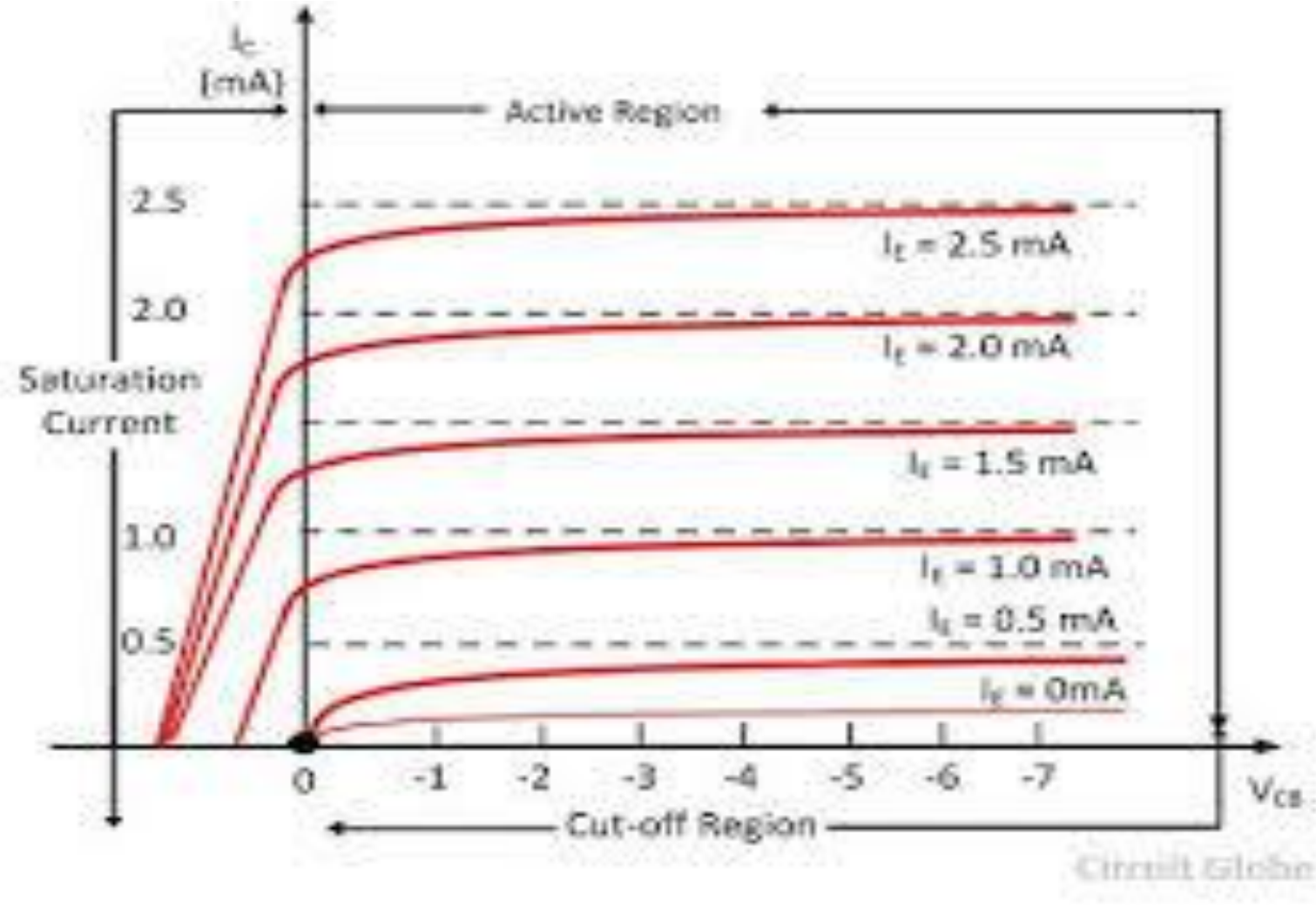
- To draw the graph in active region equation of output current,

$$I_C = \alpha I_E + I_0$$

Output V/I Characteristics of CB Configuration

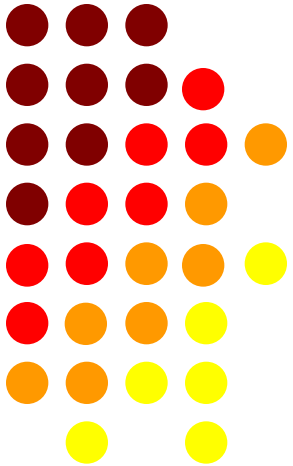
- **Active Region:** For given α and I_E, I_C is dependent only on I_0 which is slightly dependent on V_{CB}. So, graph of active region is almost independent of V_{CB}.
- **Saturation Region**: When the transistor is switched from active to saturation region, a large change in collector current for very small forward bias voltage at collector to base junction is obtained in negative direction.
- **Cut-Off Region:** When both the junctions are reverse biased, a very small collector current is obtained which is close to horizontal axis.

Output V/I Characteristics of CB Configuration



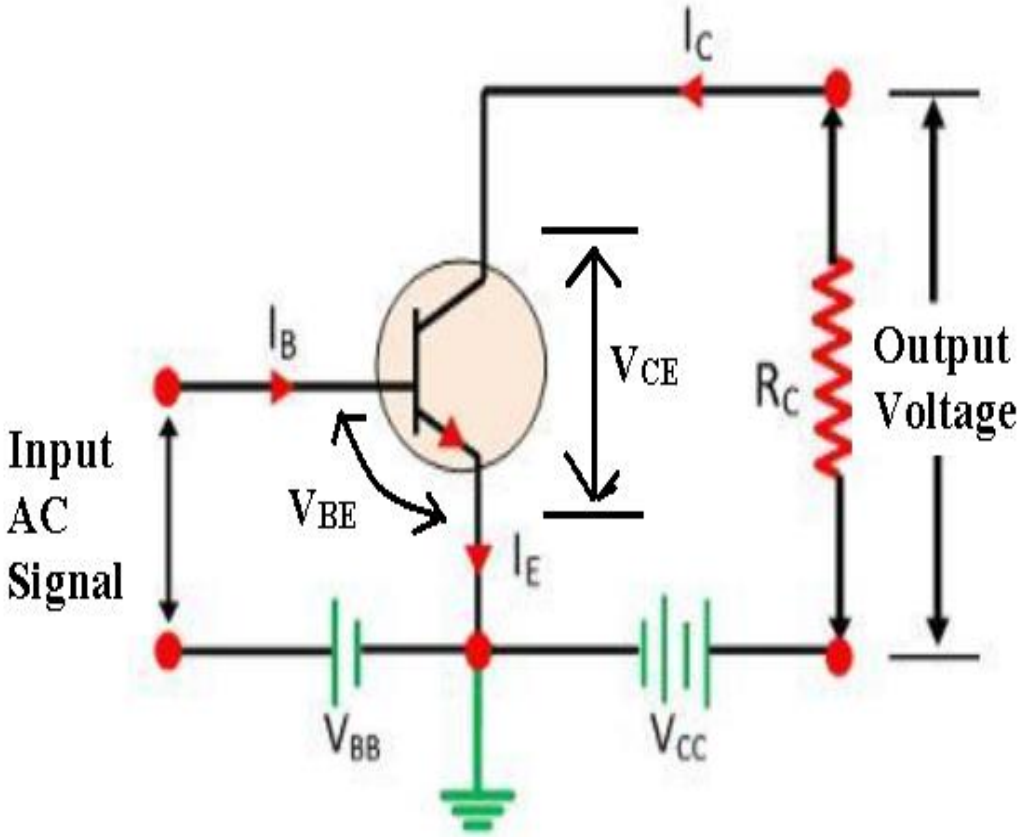
Lecture 17

CE configuration: Structure, Current gain, Input characteristics



Common Emitter Configuration (CE)

In this configuration input is applied between base and emitter while output is taken out from collector and emitter. So, emitter of transistor is common to both input and output.



i) DC Current gain:

- It is the ratio of output current (I_C) to the input current (I_B).

$$\beta = \frac{I_C}{I_B}$$

- Since value of $I_B << I_C$. So $\beta >> 1$. Therefore, current gain is available in CE configuration

- Value of β varies from 20 to 500.

Expression for Output Current

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha(I_C + I_B) + I_{CBO}$$

$$[I_E = I_C + I_B]$$

$$I_C = \alpha I_C + \alpha I_B + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \frac{I_{CBO}}{1-\alpha} \ldots\ldots\ldots 1$$

$$but \ \frac{\alpha}{1-\alpha} = \beta$$

$$\frac{\alpha}{1-\alpha} + 1 = \beta + 1$$

$$\frac{1}{1-\alpha} = \beta + 1 \ldots\ldots\ldots\ldots\ldots 2$$

Using equation 1 and 2

$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$

$$\boxed{I_C = \beta I_B + I_{CEO}}$$

Where I_{CEO}: Collector to emitter current when base is open and I_{CEO} is given by

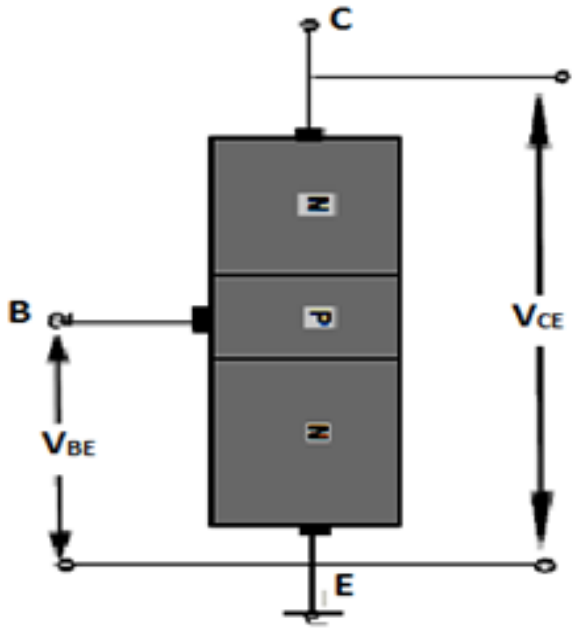
$$\boxed{I_{CEO} = (\beta + 1) I_{CBO}}$$

Input V/I Characteristics of CE Configuration

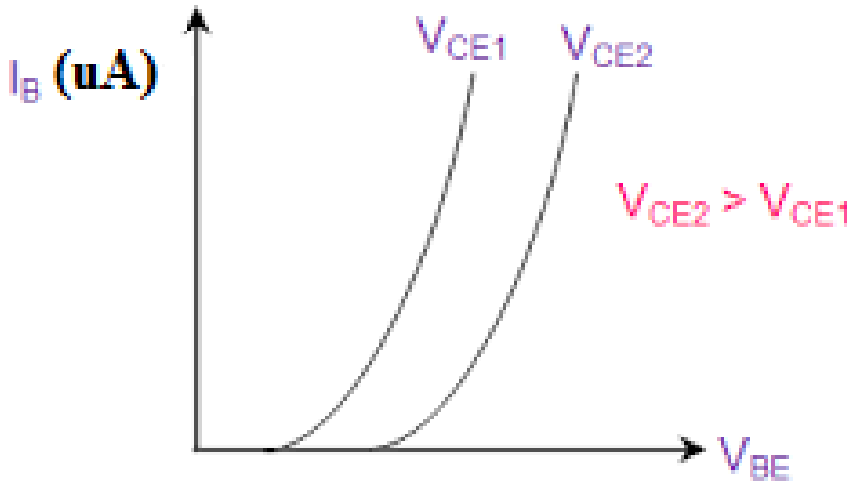
- It is graph between input current (I_B) and input voltage (V_{BE}) at constant output voltage (V_{CE}). This graph is drawn for active region of BJT.
- By keeping constant V_{CE}, when forward bias at emitter base junction is increased then graph between I_E and V_{BE} is similar to forward characteristics of pn junction diode.

Input V/I Characteristics of CE Configuration

- If this graph is again drawn for some higher value of V_{CE} a similar graph is obtained with increased knee voltage. This is due to reduction in I_B on increasing reverse bias at collector base junction.



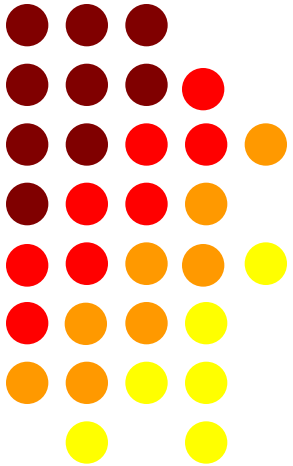
Input V/I Characteristics of CE Configuration



Input Characteristics for CE Configuration

Lecture 18

Output characteristics of CE Configuration, Comparison between different configurations of BJT on the basis of different parameters, Numerical based on BJT



Output V/I Characteristics of CE Configuration

- It is graph between output current I_C and output voltage V_{CE} at constant input current I_B. This graph is drawn for all three operating regions of BJT.

- To draw the graph in active region equation of output current,

$$I_C = \beta I_B + (\beta + 1) I_0$$

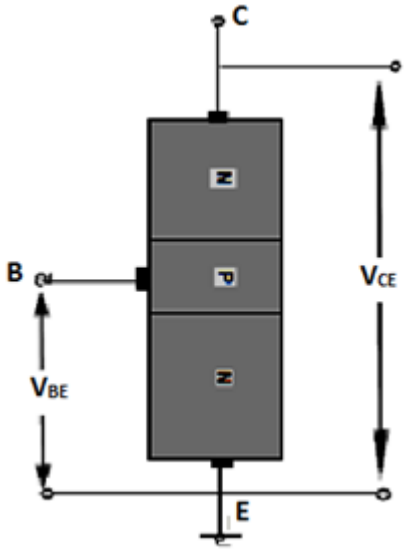
Output V/I Characteristics of CE Configuration

- **Active Region:** For given β and I_B, I_C is dependent on $(\beta + 1)I_0$ which is more dependent on V_{CE} than in case of CB configuration. So, graph of active region has some slope showing change in I_C on changing V_{CE}.

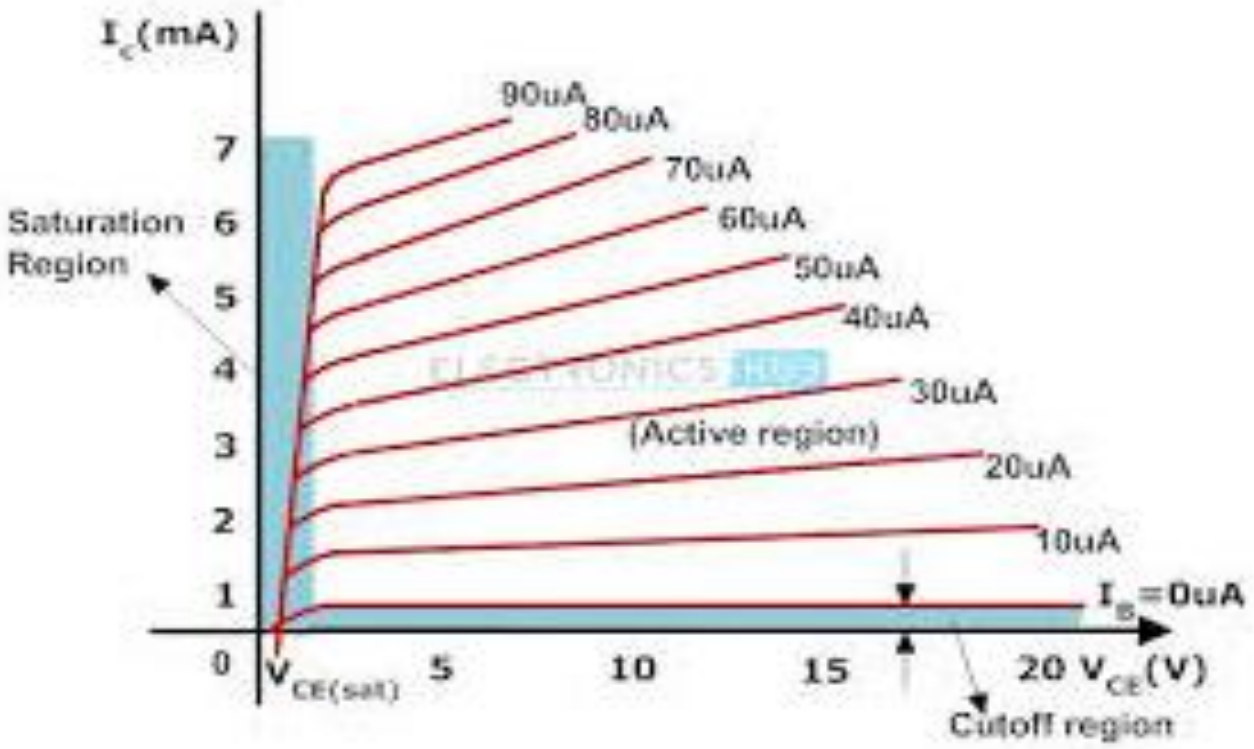
- **Saturation region:** When the transistor is switched from active to saturation region, a large change in collector current for very small change in collector voltage is obtained in negative direction.

- **Cut-Off Region**: When both the junctions are reverse biased, a very small collector current is obtained which is close to horizontal axis.

Output V/I Characteristics of CE Configuration



Output V/I Characteristics of CE Configuration



Relation between α and β

$$\alpha = \frac{I_C}{I_E} \quad and \; \beta = \frac{I_C}{I_B}$$

$$I_E = I_B + I_C$$

Dividing both sides by I_C

$$\frac{I_E}{I_C} = \frac{I_B + I_C}{I_C}$$

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\frac{1}{\alpha} = \frac{1+\beta}{\beta}$$

$$\alpha + \alpha\beta = \beta$$

$$\beta(1-\alpha) = \alpha$$

$$\boxed{\boldsymbol{\beta} = \frac{\boldsymbol{\alpha}}{1-\boldsymbol{\alpha}}}$$

Comparison of Transistor Configuration or Connections

S. No.	Characteristic	Common base	Common emitter	Common collector
1.	Input resistance	Low (about 100 Ω)	Low (about 750 Ω)	Very high (about 750 kΩ)
2.	Output resistance	Very high (about 450 kΩ)	High (about 45 kΩ)	Low (about 50 Ω)
3.	Voltage gain	about 150	about 500	less than 1
4.	Applications	For high frequency applications	For audio frequency applications	For impedance matching
5.	Current gain	No (less than 1)	High (β)	Appreciable

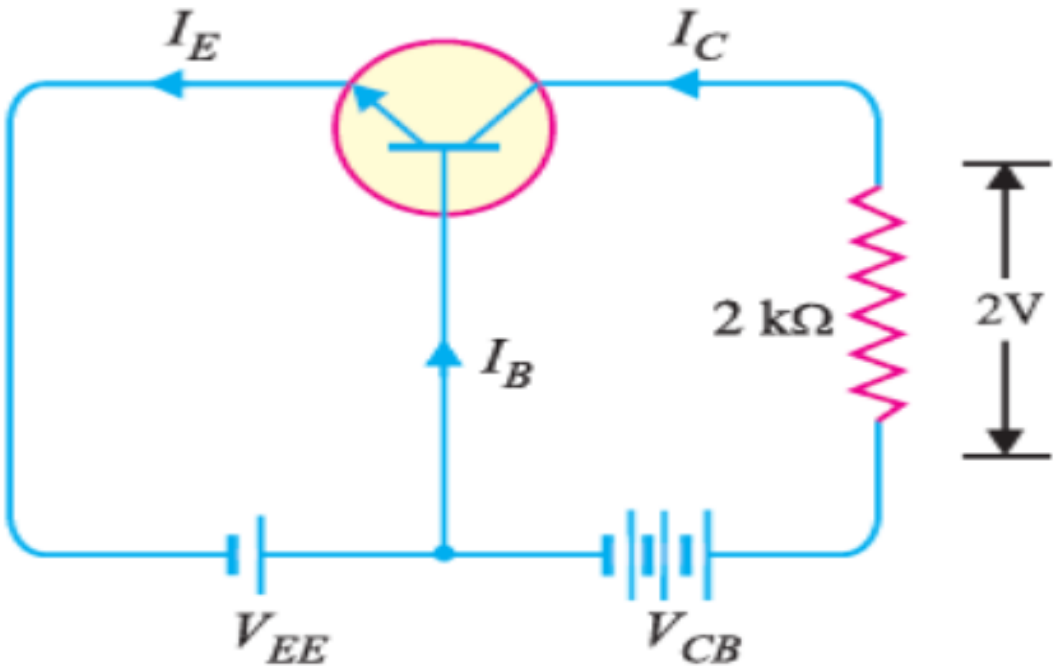
Ques-1 In a common base connection, the emitter current is 1mA. If the emitter circuit is open, the collector current is 50 µA. Find the total collector current. Given that α = 0.92.

$$\text{Here, } I_E = 1\text{ mA}, \alpha = 0.92, \quad I_{CBO} = 50\ \mu\text{A}$$

$$\therefore \quad \text{Total collector current, } I_C = \alpha I_E + I_{CBO} = 0.92 \times 1 + 50 \times 10^{-3}$$

$$= 0.92 + 0.05 = \mathbf{0.97\ mA}$$

Ques-2: In a common base connection, α = 0.95. The voltage drops across 2 kΩ resistance which is connected in the collector is 2V. Find the base current.



The voltage drop across RC (= 2 kΩ) is 2V.

$$\therefore \quad I_C = 2\,\text{V}/2\,\text{k}\Omega = 1\,\text{mA}$$

Now $\alpha = I_C/I_E$

$$\therefore \quad I_E = \frac{I_C}{\alpha} = \frac{1}{0.95} = 1.05\,\text{mA}$$

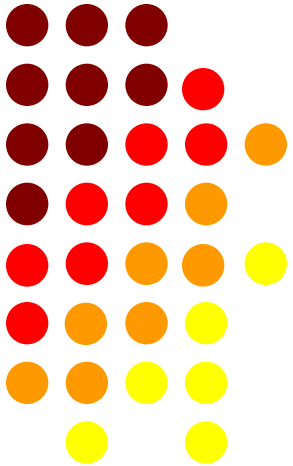
Using the relation, $I_E = I_B + I_C$

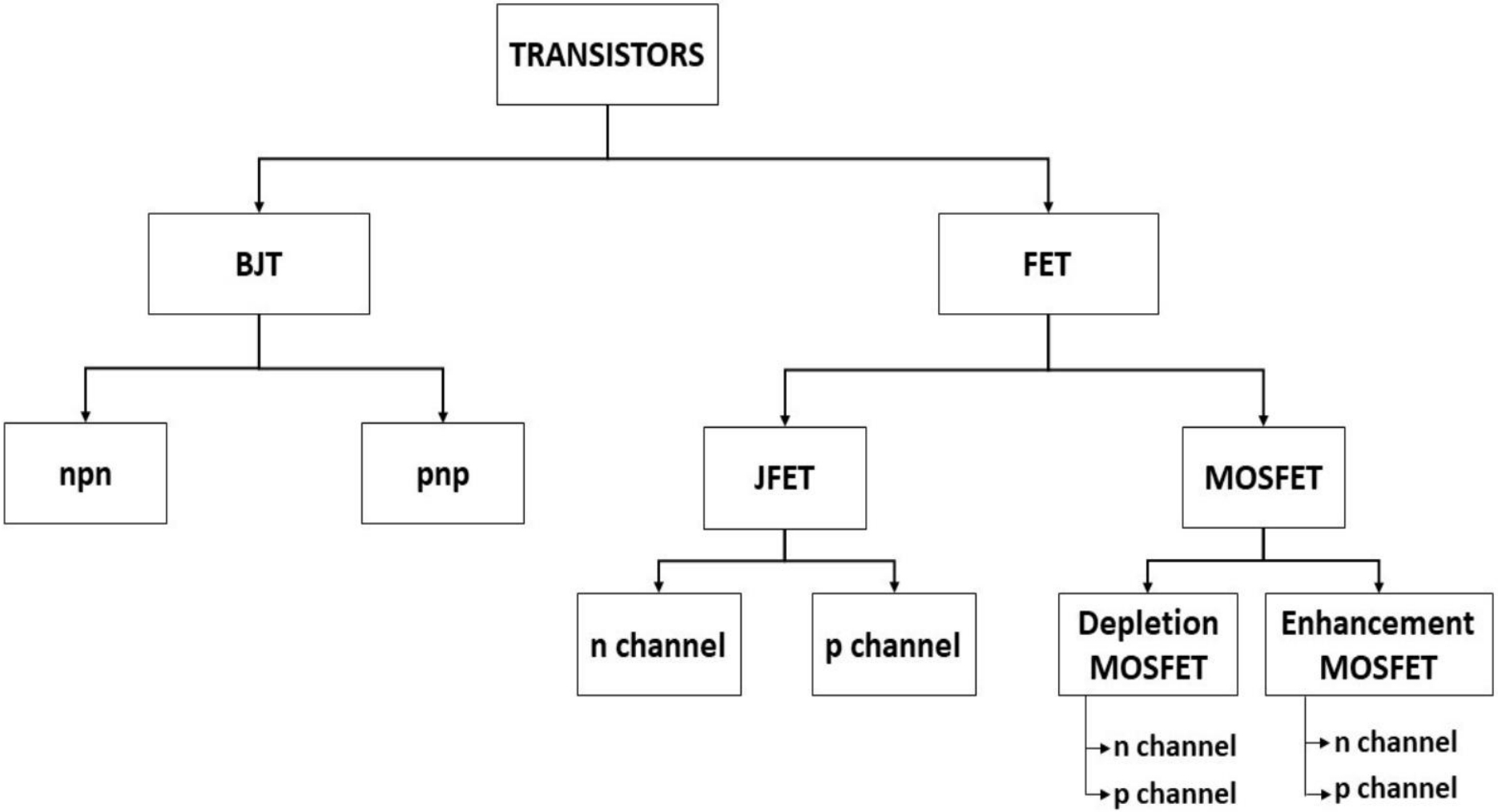
$$\therefore \quad I_B = I_E - I_C = 1.05 - 1$$

$$= 0.05\,\text{mA}$$

Lecture 19

Introduction of FET,
Classification of FET,
Introduction of JFET, Output and Transfer characteristics of n channel JFET




TRANSISTORS
BJT
FET
npn
pnp
JFET
MOSFET
n channel
p channel
Depletion MOSFET
Enhancement MOSFET
n channel
p channel
n channel
p channel

BJT has two principle disadvantage

- It has low input impedance due to Forward biased emitter junction.
- It has considerable noise level.
- The above problem are overcome by:
- FET has large input impedance by virtue of its construction and biasing.
- FET is generally much less noisy than BJT

Remember:

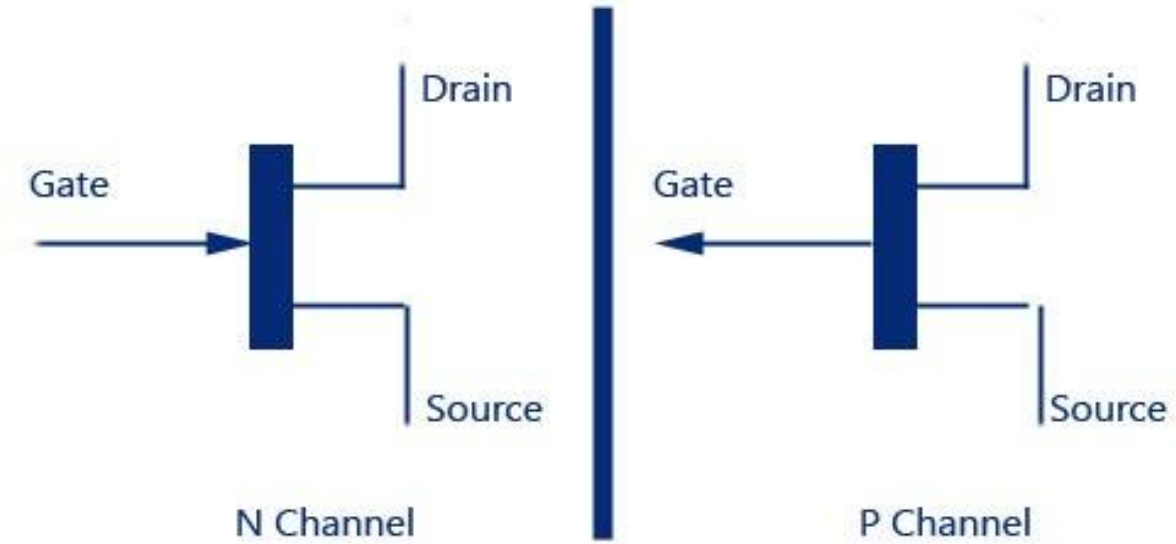
BJT is a current controlled device

FET is a Voltage controlled device.

Introduction of FET

- A **field-effect transistor** (FET) is a three terminal (namely drain, source and gate) semiconductor device in which current conduction is by only one type of majority carriers (electrons in case of an N-channel FET or holes in a P-channel FET)

- It is also sometimes called the uni-polar transistor.



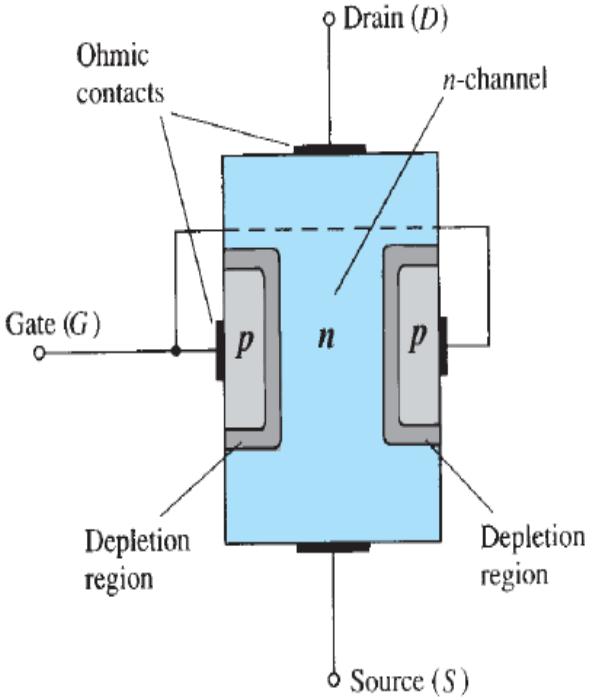
FET

Field Effect Transistor FET

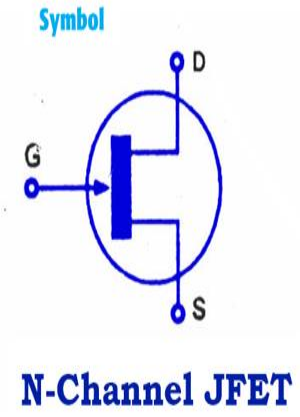
N- Channel JFET(Junction Field Effect Transistor)

Construction:

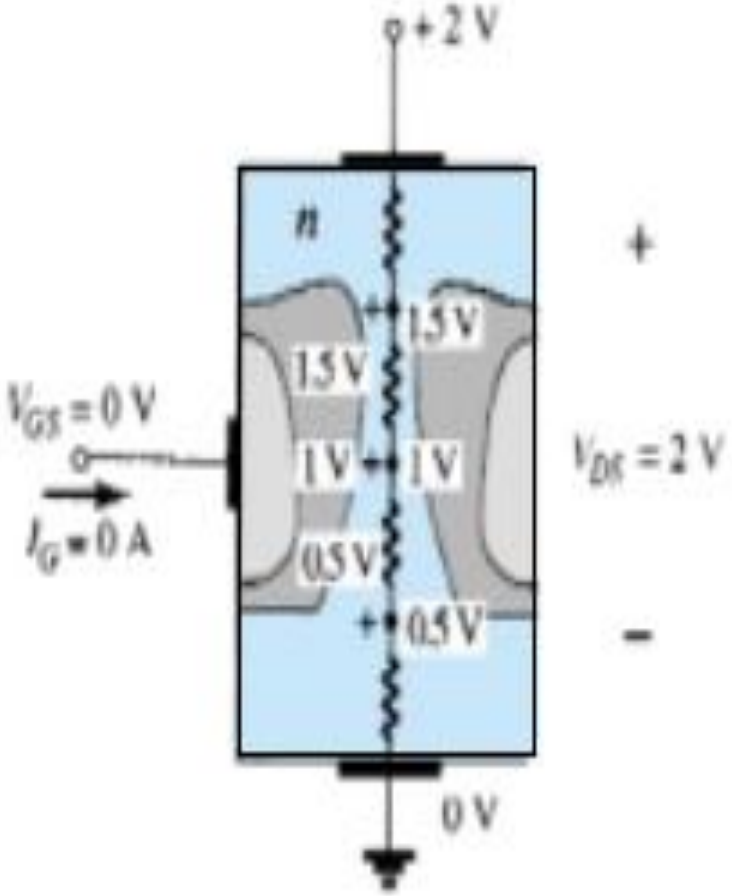
- A n-channel JFET have n type base.
  - On both side of base two heavily doped p regions are formed.
  - So two p-n junction is formed which are internally connected by a gate terminal. Other two terminal are drain and source.



Junction field-effect transistor (JFET).



- In JFET structure, the channel is uniformly doped and it can be modeled as series combination of equal resistances.
- If current is flowing from drain to source, the voltage at upper part of the channel is higher than the lower part.
- So if we apply $V_{Ds} > 0$ and V_{GS} 0, both pn junctions are reverse biased and very high input impedance is achieved.
- This reverse bias voltage is not uniform and decreases as we move downwards.
- So, a non uniform depletion region is formed at junctions which is wider in upper part than the lower part of the channel.



Working of n Channel JFET

Its working is divided in two parts:

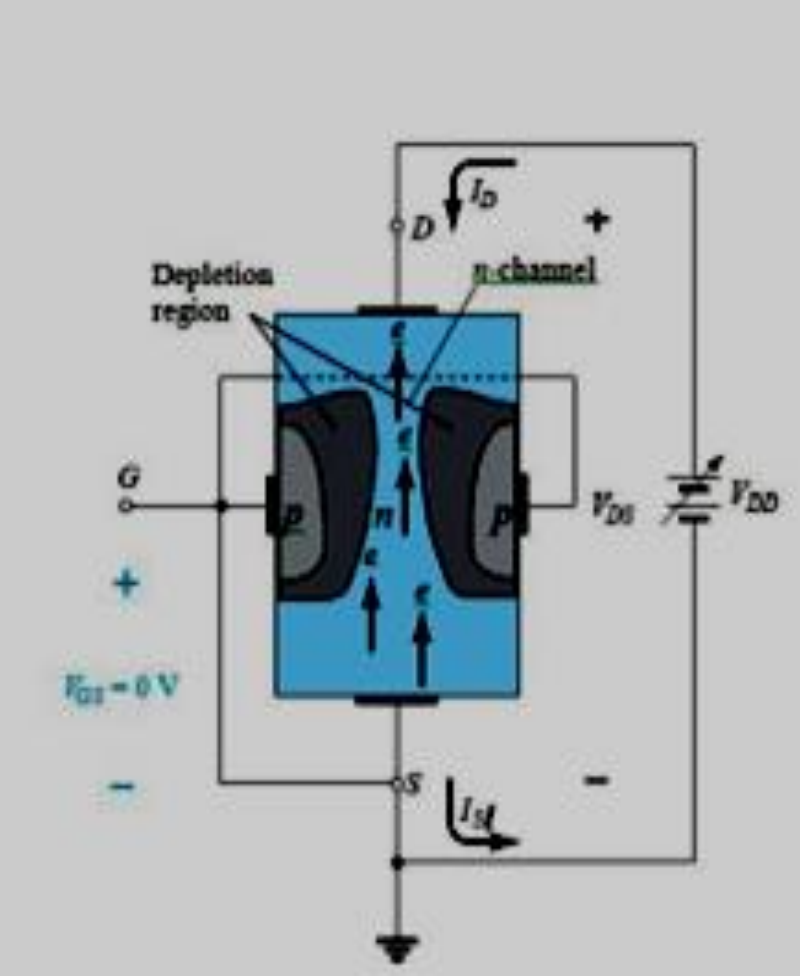
(1) When **V_{DS}>0 and V_{GS}=0**

(2) When **V_{DS}>0 and VGS<0**

1. When V_{DS}>0 and V_{GS}=0:

- Two pn junctions are reverse biased and biasing voltage is decreasing from top to bottom. So depletion is more on upper part of the structure than lower part.
- Electrons in channel move towards drain (positive terminal), so a current I_D from drain to source us obtained
- On increasing V_{DS}, I_D as well as reverse bias both increases

Working of n Channel JFET



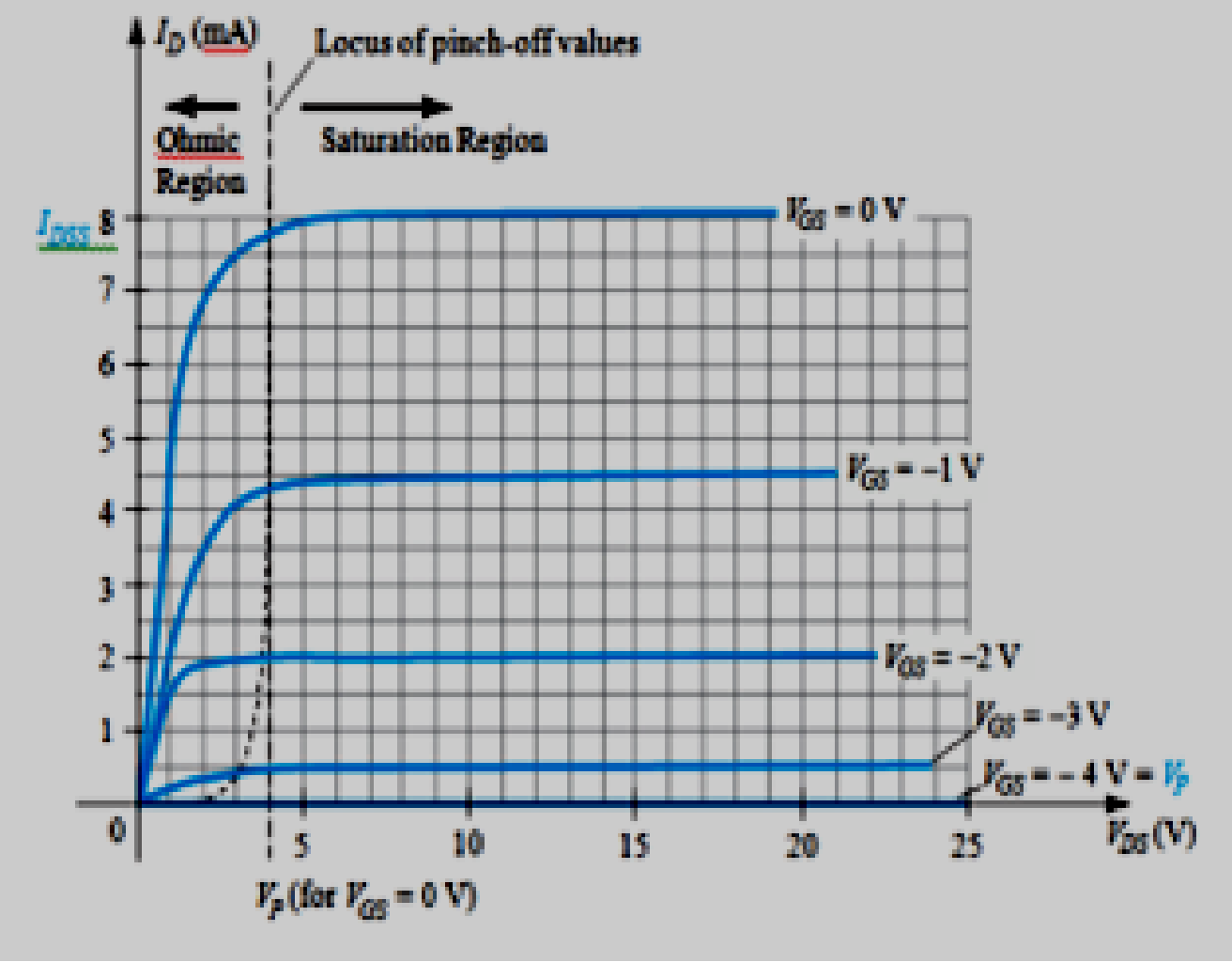
Working of n Channel JFET

- At certain value of V_{DS}, width of depletion layer become maximum and drain current become constant. It is called pinch off condition
- V_{DS} corresponding to pinch-off condition is called pinch off voltage (V_P) and constant drain current is denoted as I_{DSS}.
- After V_{DS}= V_P, on increasing $V_{DS,}$ I_D remains constant until reverse breakdown.
- This condition is shown in graph of I_D vs V_{DS} at V_{GS}=0V.

(2) When V_{DS}>0 and V_{GS}<0

- Now pinch off condition arrives at lower values of V_{DS}
- The magnitude of saturation current is also smaller than the magnitude at V_{GS}=0V.
- This condition is shown graphically for different negative values of V_{GS}

Working of n Channel JFET (Drain Characteristics)



Output Characteristics (Drain Characteristics)

- It is graph between output current I_D and output voltage V_{DS} at constant V_{GS}. It can be explained from working of the structure discussed above.
- For smaller values of V_{DS}, $I_D \propto V_D$. So this region of the graph is called ohmic or linear region.
- In ohmic region the slope of the graph is dependent on V_{GS}. So FET can be used as voltage controlled resistance.
- After pinch off condition the drain current become constant and this region of the graph is called saturation region.

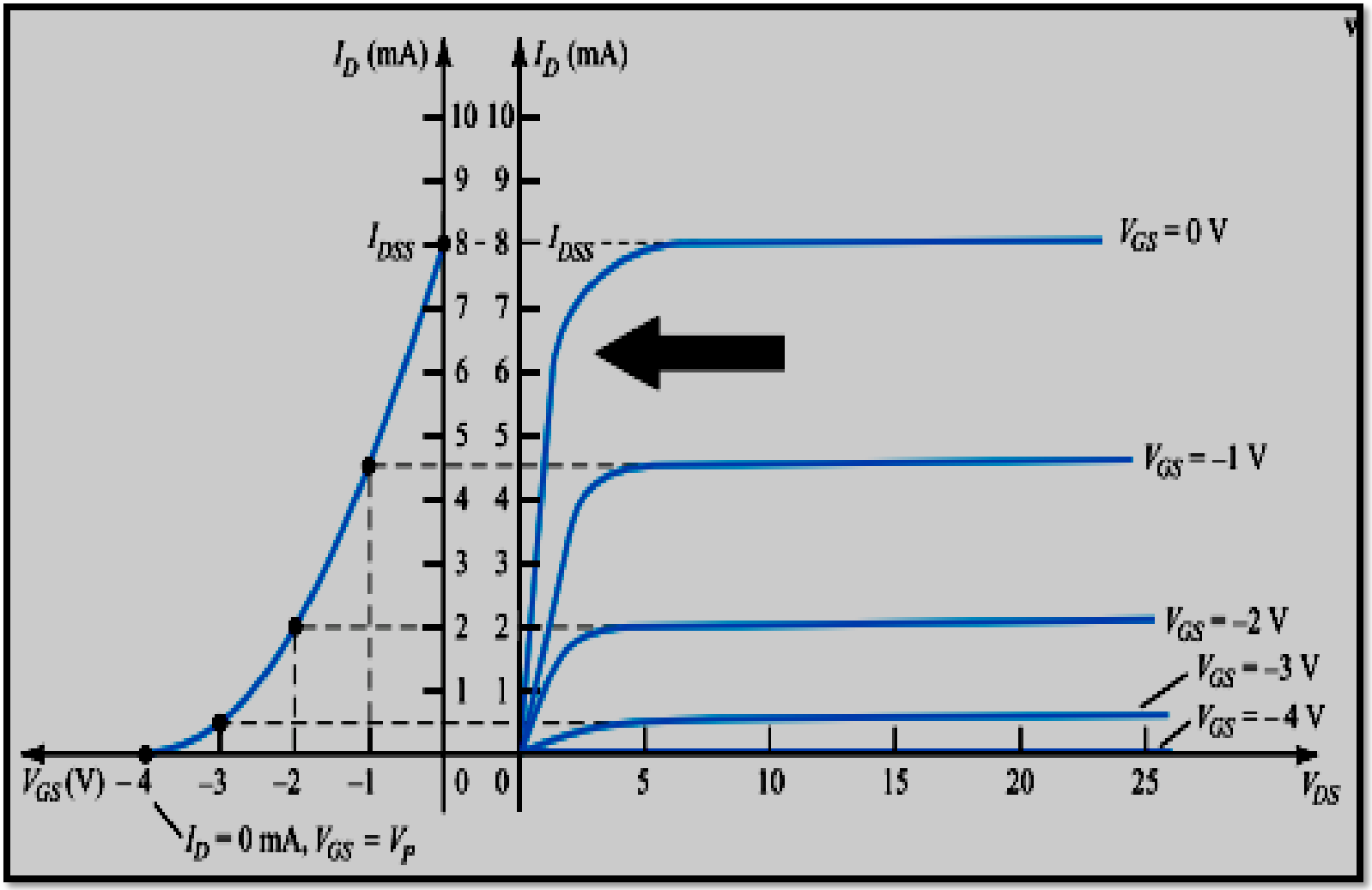
Transfer Characteristics

- It is graph between output current I_D and input voltage V_{GS}.
- The relation between I_D and V_{GS} can be given as:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

- Above equation is also known as Shockley's equation.
- The transfer curve can be obtained using Shockley's equation or from the output characteristics.

Transfer Characteristics



Transfer Characteristics

- Here two graphs are provided, with the vertical scaling in milliamperes for each graph. One is a plot of I_D versus V_{DS} , while the other is I_D versus V_{GS} .
- Using the drain characteristics on the right of the “y” axis, a horizontal line can be drawn from the saturation region of the curve denoted V_{GS} =0 V to the I_D axis. The resulting current level for both graphs is I_{DSS}.
- In a similar way for different values of V_{GS} we can note constant values of I_D from output curve.
- By joining all these points curve obtained is called transfer curve.

Transfer characteristics (From Schokley Equation)

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

- Let $I_{DSS} = 8\ mA$, $V_P = -4\ V$

a) $V_{GS} = 0V$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 8\left(1 - \frac{0}{-4}\right)^2 = 8\ mA$$

b) $V_{GS} = -1V$

$$I_D = 8\left(1 - \frac{-1}{-4}\right)^2 = 4.5\ mA$$

c) $V_{GS} = -2V$

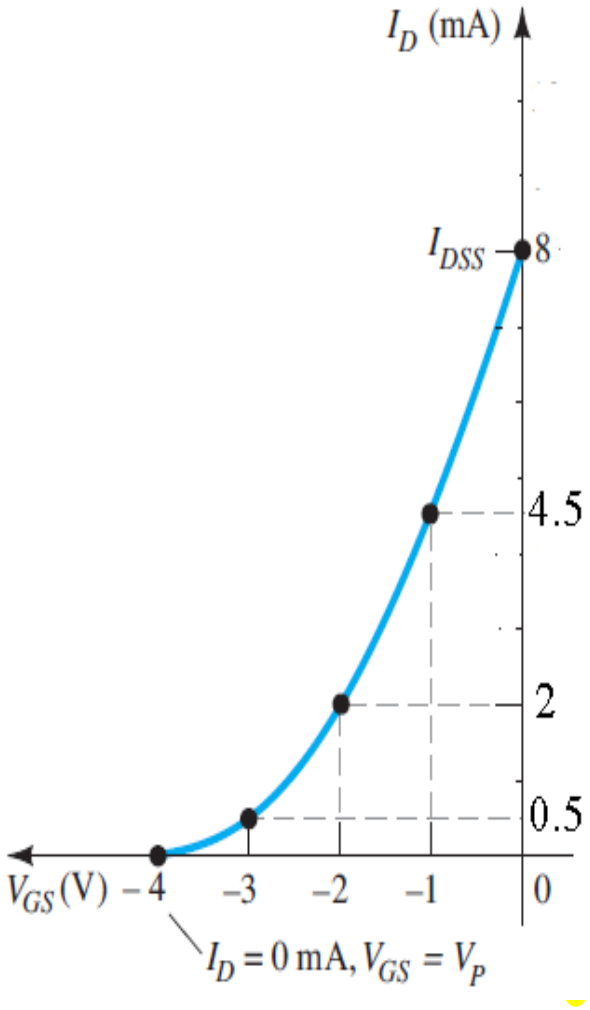
$$I_D = 8\left(1 - \frac{-2}{-4}\right)$$

d) $V_{GS} = -3V$

$$I_D = 8\left(1 - \frac{-3}{-4}\right)$$

e) $V_{GS} = -4V$

$$I_D = 8\left(1 - \frac{-4}{-4}\right)$$



Lecture 20

Use of JFET as VVR,
Different parameters of JFET,
Introduction of DMOSFET,
Output and Transfer characterics of DMOSFET

FET as a Voltage Variable Resistor-(VVR):

- FET is a device that is usually operated in the constant-current portion of its output characteristics.
- But if it is operated on the region prior to pinch-off (that is where VDS is small, say below 100 mV), it will behave as a voltage-variable resistor (WE).
- It is due to the fact that in this region drain-to-source resistance RDS can be controlled by varying the bias voltage VGS.
- In such applications the FET is also referred to as a voltage-variable resistor or volatile dependent resistor.

JFET as a voltage variable resistance (VVR) or voltage controlled resistance

JFET works as a variable resistance in ohmic region. The resistance of JFET is given by:

$$r_d = \frac{r_O}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

Where:

r_o = 10 KΩ (Resistance at V_{GS} = (

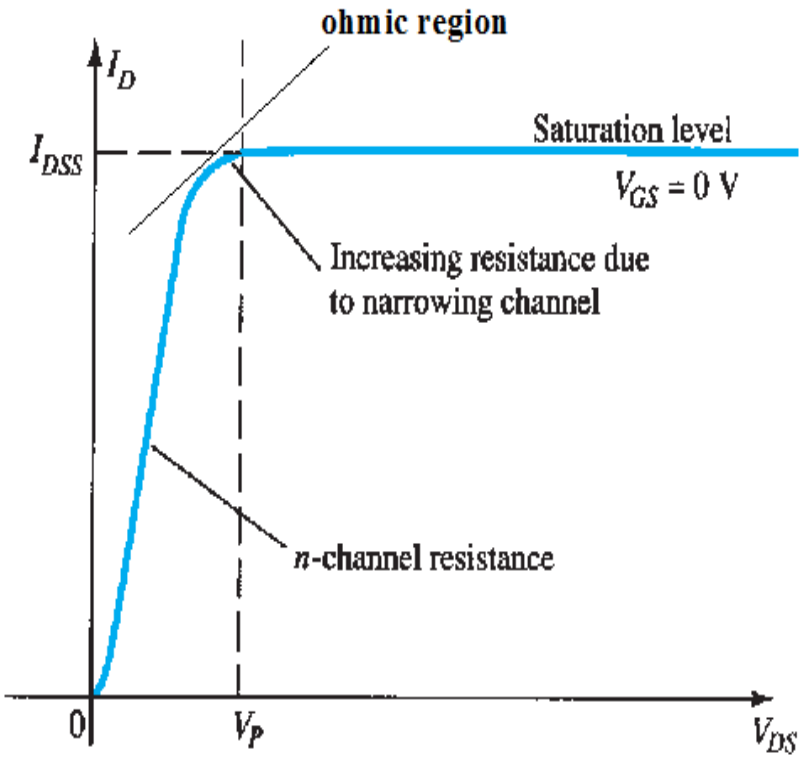
i) At V_{GS} = 0

$$r_d = \frac{10}{\left(1 - \frac{0}{-4}\right)^2} = 10K\Omega$$

ii) At V_{GS} = -2

$$r_d = \frac{10}{\left(1 - \frac{-2}{-4}\right)^2} = 13.33K\Omega$$

So JFET works as variable resistance or voltage-controlled resistance.



Different parameters of JFET

- Transconductance (g_m)
- Dynamic Output Resistance
- Amplification Factor

Transconductance (g_m) and Its Expression

- Transconductance (g_m): It is defined the ratio of change in drain current (ΔI_D) and change in gate to source voltage (ΔV_{GS}) at constant drain to source voltage (V_{DS}).
- Unit of g_m is Siemen.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \Big| \; V_{DS} = Constant$$

$$= \frac{dI_D}{dV_{GS}}$$

Expression for transconductance (g_m):

From Shockley equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \text{----------1}$$

Differentiating equation 1 with respect to V_{GS}

$$\frac{dI_D}{dV_{GS}} = I_{DSS}\, X\, 2\left(1 - \frac{V_{GS}}{V_P}\right)\left(\frac{1}{V_P}\right)$$

$$But \quad g_m = \frac{dI_D}{dV_{GS}}$$

$$SO\ g_m = -\frac{2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right) \ldots\ldots\ldots 2$$

$$From\ equation\ 1 \qquad \left(1 - \frac{V_{GS}}{V_P}\right) = \sqrt{\frac{I_D}{I_{DSS}}} \ldots\ldots 3$$

$$Using\ 2\ and\ 3 \qquad g_m = -\frac{2I_{DSS}}{V_P}\sqrt{\frac{I_D}{I_{DSS}}}$$

$$\boxed{g_m = \frac{2}{V_P}\sqrt{I_{DSS} I_D}}$$

Dynamic Output Resistance

- This is the ratio of change of drain to source voltage (δV_{DS}) to the change of drain current (δI_D) at a constant gate to source voltage (V_{GS} = Constant). The ratio is denoted as r_d.

$$r_d = \frac{\delta V_{DS}}{\delta I_D} \quad at\ constant\ \ V_{GS}$$

Amplification Factor

- The amplification factor is defined as the ratio of change of drain voltage (δV_{DS}) to change of gate voltage (δV_{GS}) at a constant drain current (I_D = Constant).

$$\mu = \frac{\delta V_{DS}}{\delta V_{GS}} \quad at\ constant\ \ I_D$$

- There is a relation between transconductance (g_m) and dynamic output resistance (r_d) and that can be established in the following way.

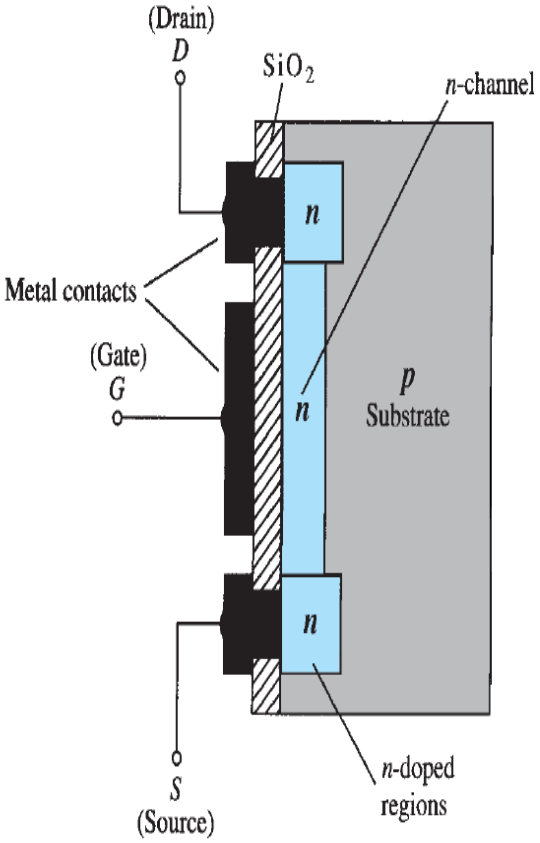
$$\mu = \frac{\delta V_{DS}}{\delta V_{GS}} = \frac{\delta V_{DS}}{\delta I_D} \times \frac{\delta I_D}{\delta V_{GS}}$$

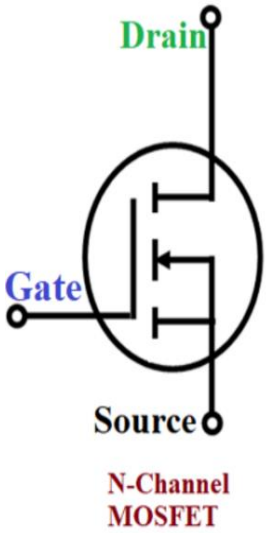
$$\Rightarrow \mu = r_d \times g_m$$

N-Channel Depletion Type MOSFET

Construction:

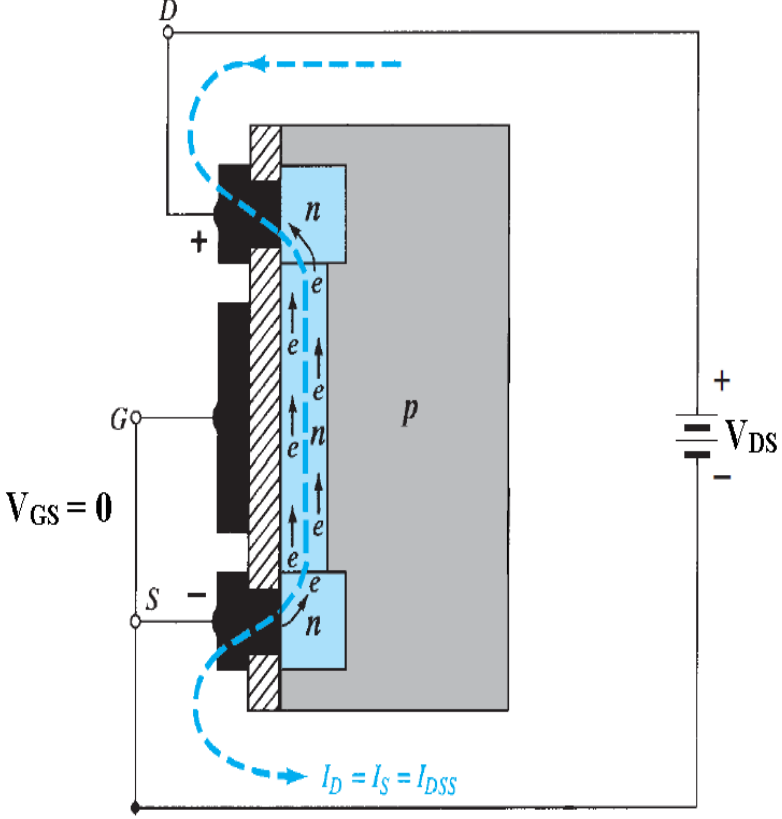
- n-channel depletion type MOSFET have p-type base(substrate). Then two n region are formed.
- A thin layer of Sio_2 (Silicon di oxide) is deposited. Drain and source are connected with metallic contact.
- A n channel is formed between two n regions. Gate is insulated from n-channel by Sio_2 layer. So, I_G is zero.

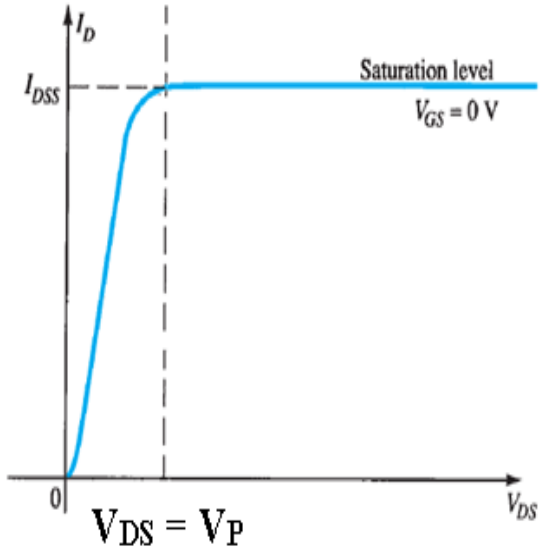




Operation:

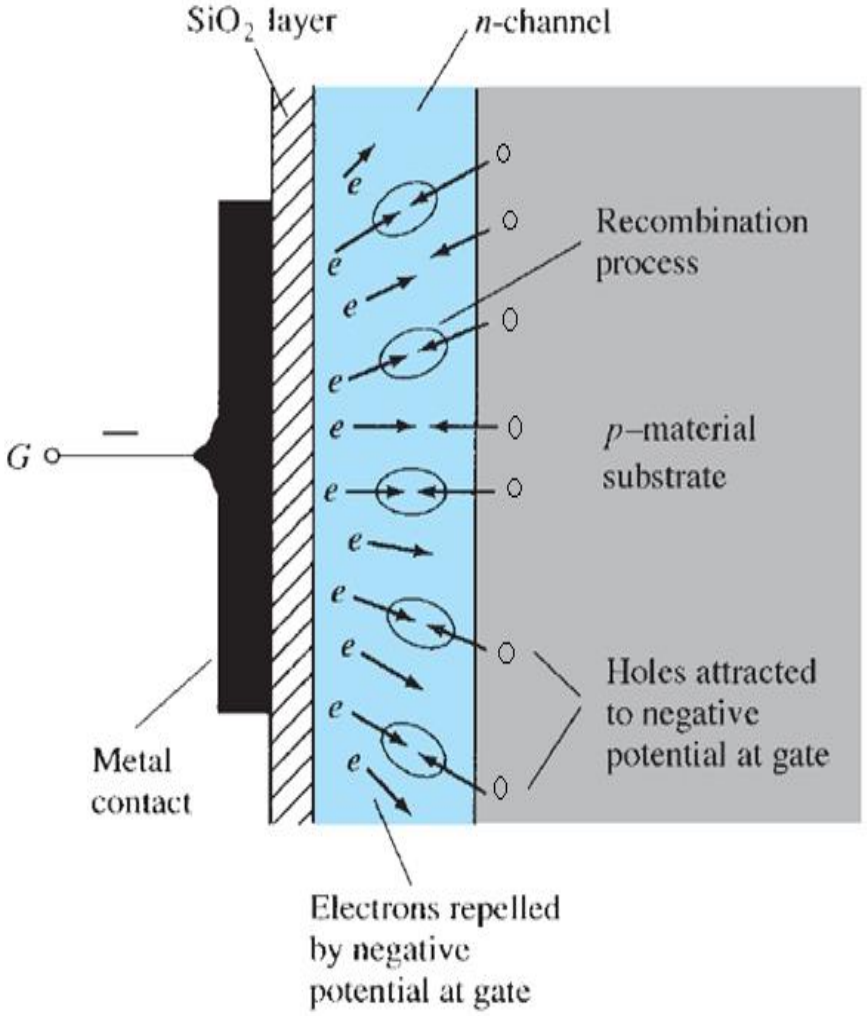
- When V_{DS} is increased more and more electrons move from source to drain. So current increases. A condition comes when current becomes cuuent.
- This condition is called pinch-off condition. The value of V_{DS} which established this condition is called pinch-off voltage (V_P). After pinch-off current becomes constant.





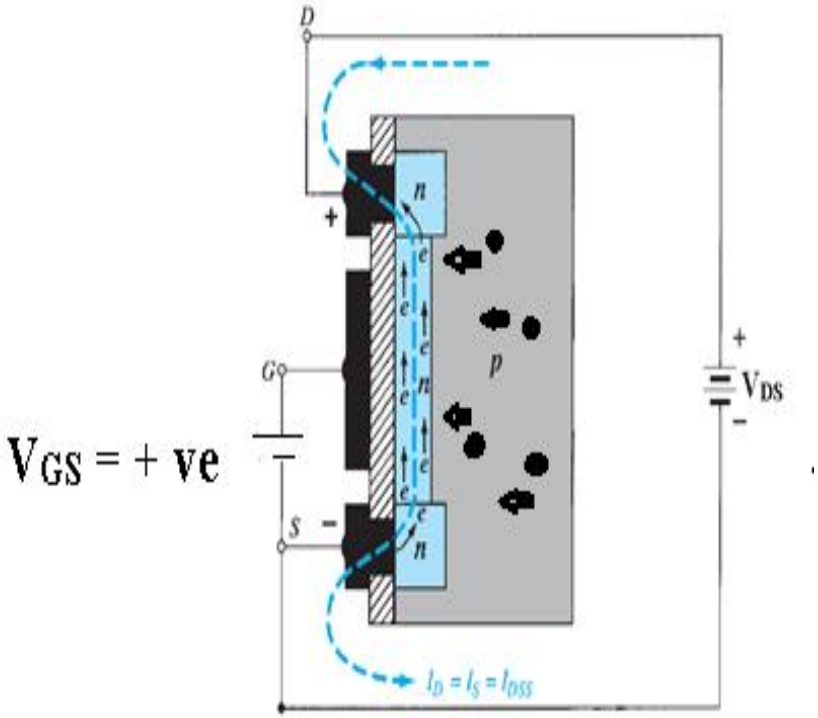
V_{DS} = +ve and V_{GS} = -ve

- If V_{GS} is increased then holes in p-type substrate moves towards the channel.
- So, recombination process occurs in channel. So, pinch-off condition comes earlier and pinch-off voltage decreases in parabolic manner. This is called depletion mode.



V_{DS} = + ve and V_{GS} = + ve

- If positive voltage is applied at gate then electrons in p-type substrate move towards the channel. So, number of electrons in channel increases. This is called enhancement mode.



Characteristics.

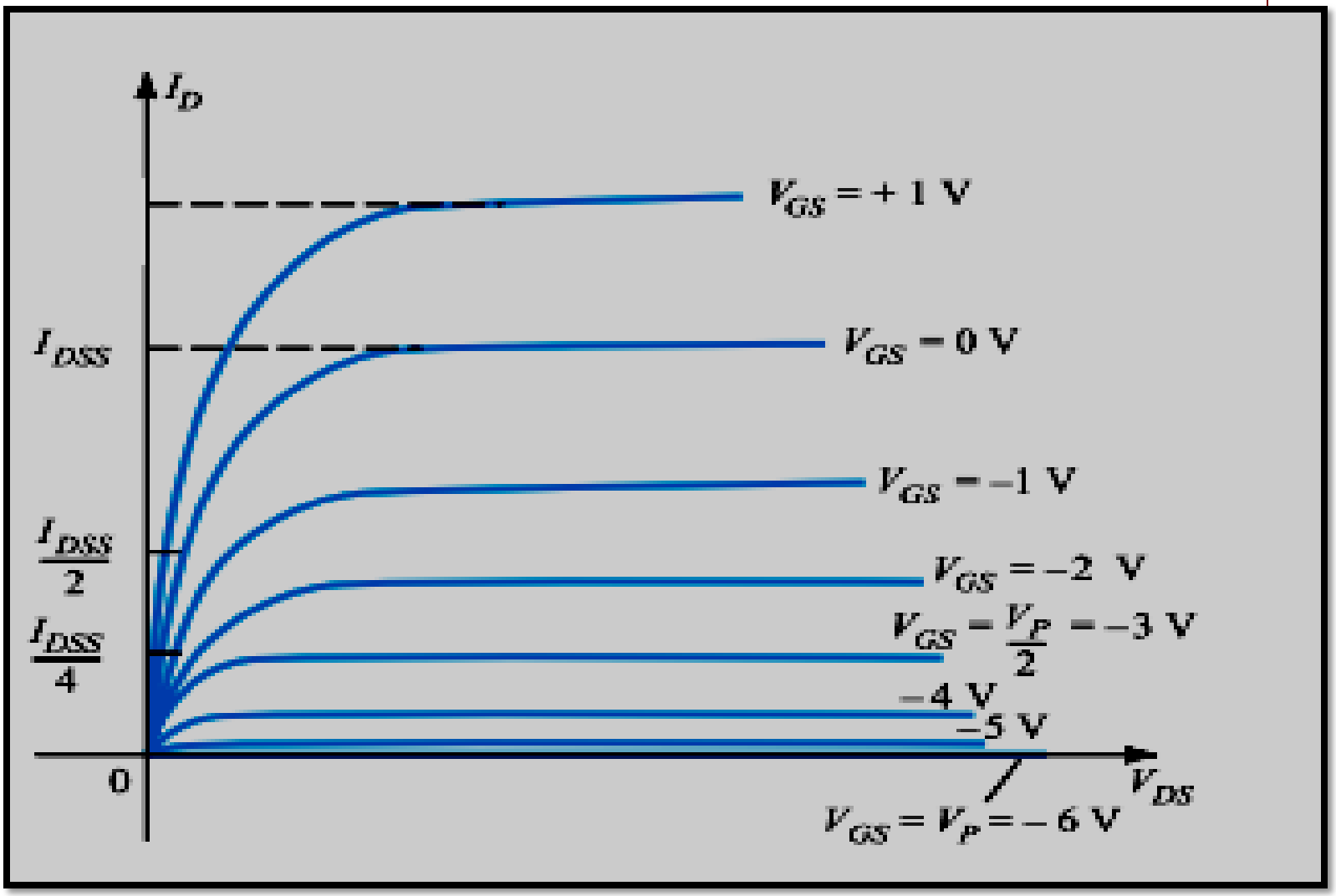
It has two types of characteristics.

i) Drain or output characteristics: It is the curve between drain current (I_D) and drain to source voltage (V_{DS}), while gate to source voltage (V_{GS}) should be constant.

ii) Transfer characteristics:

It is the curve between drain current (I_D) and gate to source voltage (V_{GS}), while drain to source voltage (V_{DS}) should be constant.

Drain or Output Characteristics



Output Characteristics (Drain Characteristics)

- It is graph between output current I_D and output voltage V_{DS} at constant V_{GS}. It can be explained from working of the structure discussed above.
- For smaller values of V_{DS}, $I_D V_{D.}$ So this region of the graph is called ohmic or linear region.
- In ohmic region the slope of the graph is dependent on V_{GS}. So MOSFET can be used as voltage controlled resistance.
- After pinch off condition the drain current become constant and this region of the graph is called saturation region.

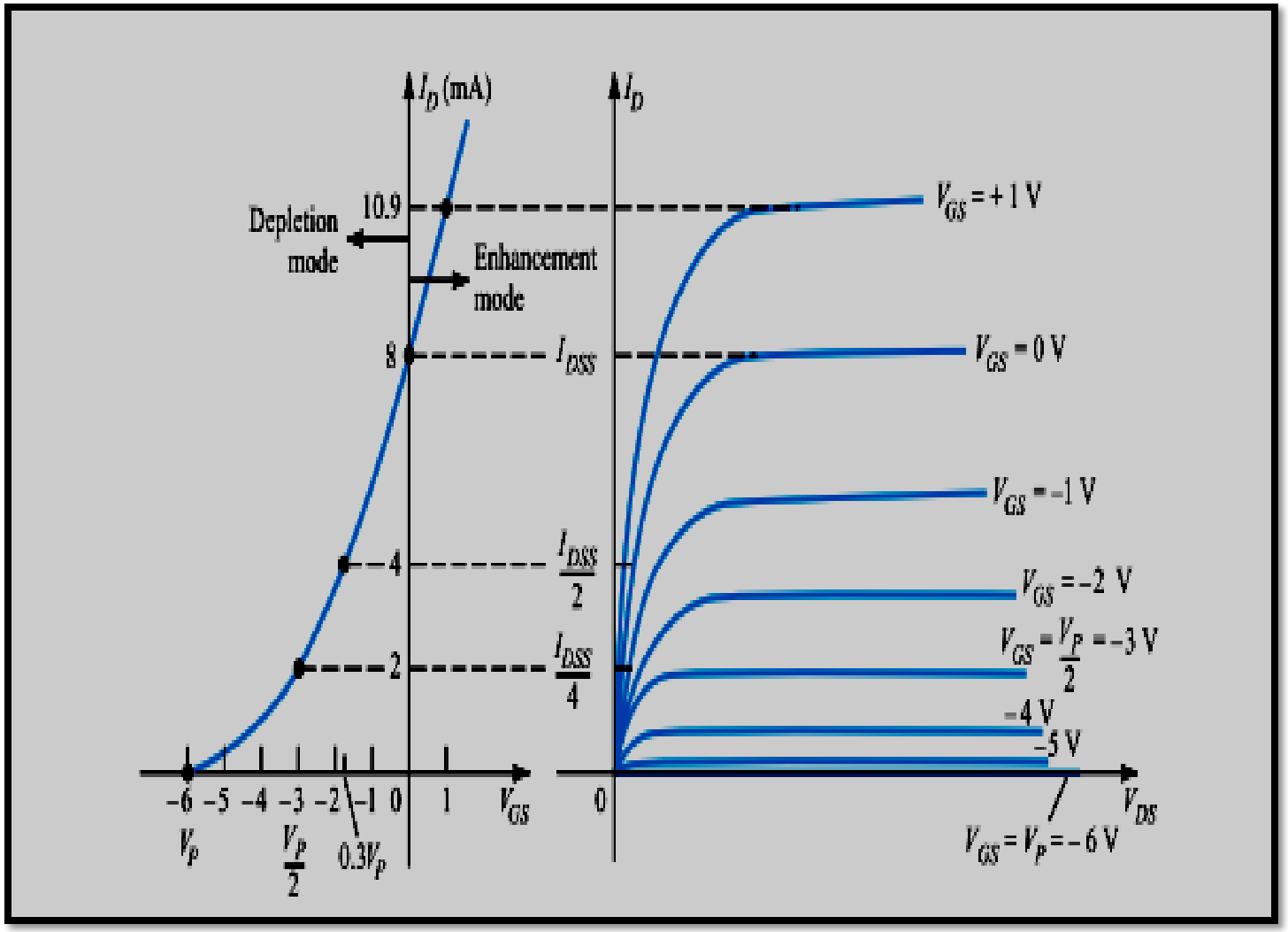
Transfer Characteristics

- It is graph between output current I_D and input voltage V_{GS}.
- The relation between I_D and V_{GS} can be given as:

$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$$

- Above equation is also known as Shockley's equation.
- The transfer curve can be obtained using Shockley's equation or from the output characteristics.

Transfer Characteristics



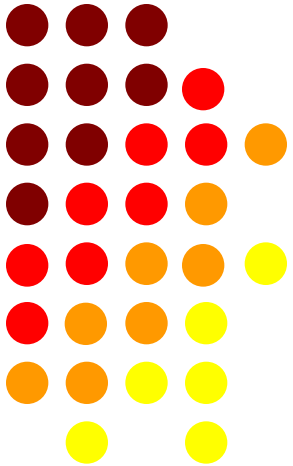
Transfer Characteristics

- Here two graphs are provided, with the vertical scaling in milliamperes for each graph. One is a plot of I_D versus V_{DS} , while the other is I_D versus V_{GS} .
- Using the drain characteristics on the right of the “y” axis, a horizontal line can be drawn from the saturation region of the curve denoted V_{GS} =0 V to the I_D axis. The resulting current level for both graphs is I_{DSS}.
- In a similar way for different values of V_{GS} we can note constant values of I_D from output curve.
- By joining all these points curve obtained is called transfer curve.

Lecture 21

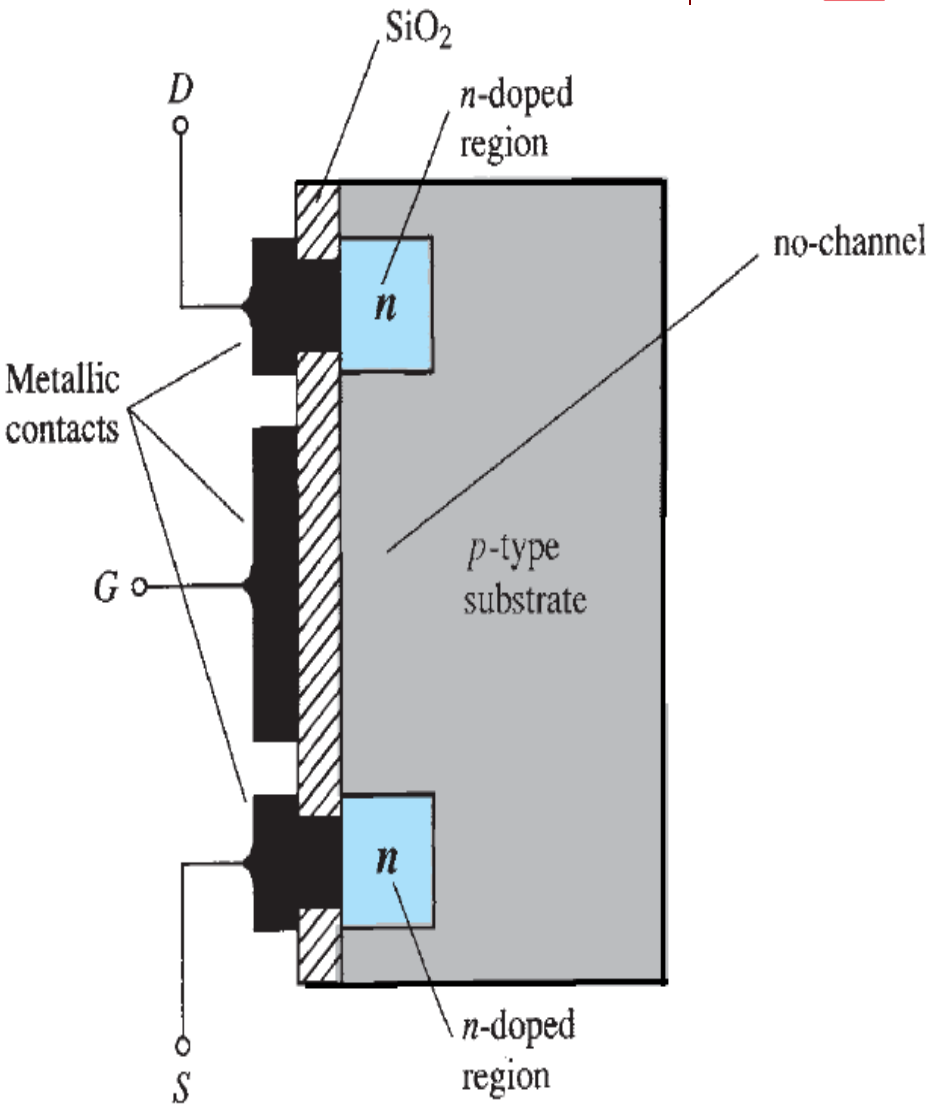
Introduction of EMOSFET and its output and transfer characteristics)

, Comparison between BJT & FET & Comparison between JFET, DMOSFET & EMOSFET



N-Channel Enhancement Type MOSFET

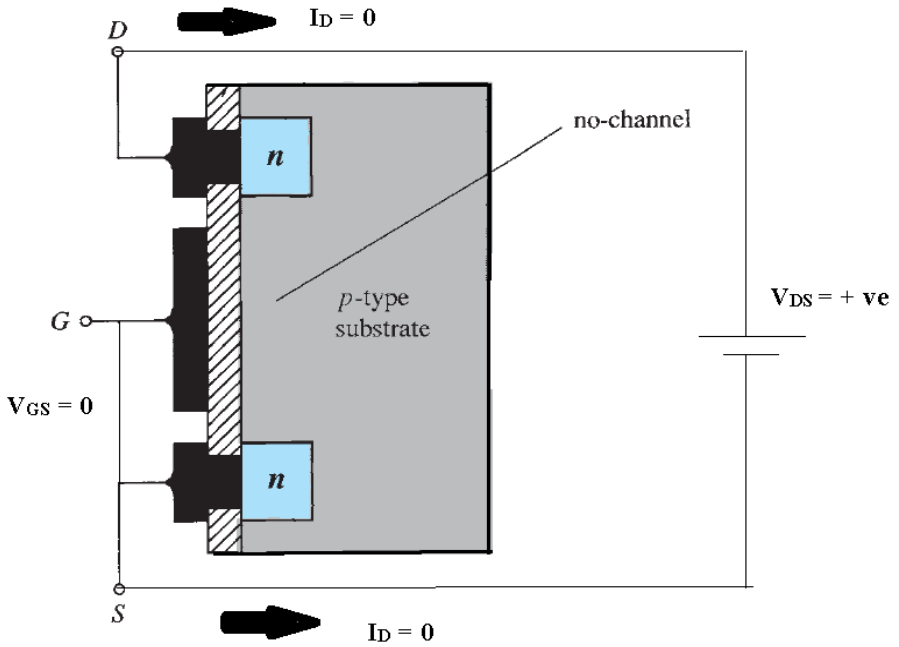
- n-channel Enhancement type MOSFET has p type substrate.
- Then two n regions are formed, A thin layer of Sio_2 (Silicon die oxide) is deposited.
- Drain and source are connected with the help of metallic contact. There is no channel between two n regions.



Operation:

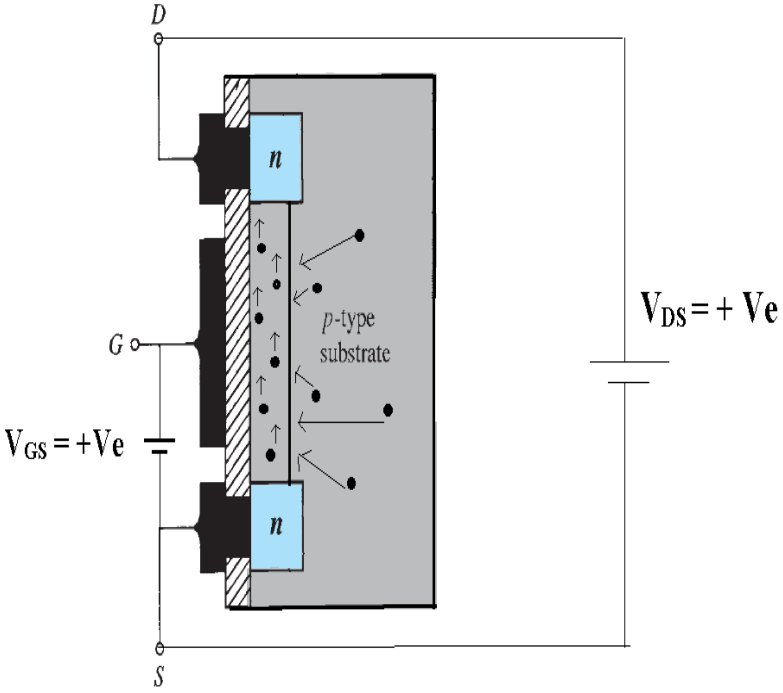
i) V_{DS} = + ve, V_{GS} = 0

- If V_{DS} is increased then no current will flow because the is no channel i.e. $I_D = 0$



ii) V_{DS} = + Ve , V_{GS} = +Ve

- If positive voltage is applied at gate then electron in p type moves towards the gate and holes moves away from the gate. Till 2V no channel is formed. But after 2V channel is formed. This 2V is called threshold voltage (V_T). If V_{GS} is further increased then I_D continuously increases. This is called enhancement MOSFET.



It has two types of characteristics.

i) **Drain or output characteristics**: It is the curve between drain current (I_D) and drain to source voltage (V_{DS}), while gate to source voltage (V_{GS}) should be constant.

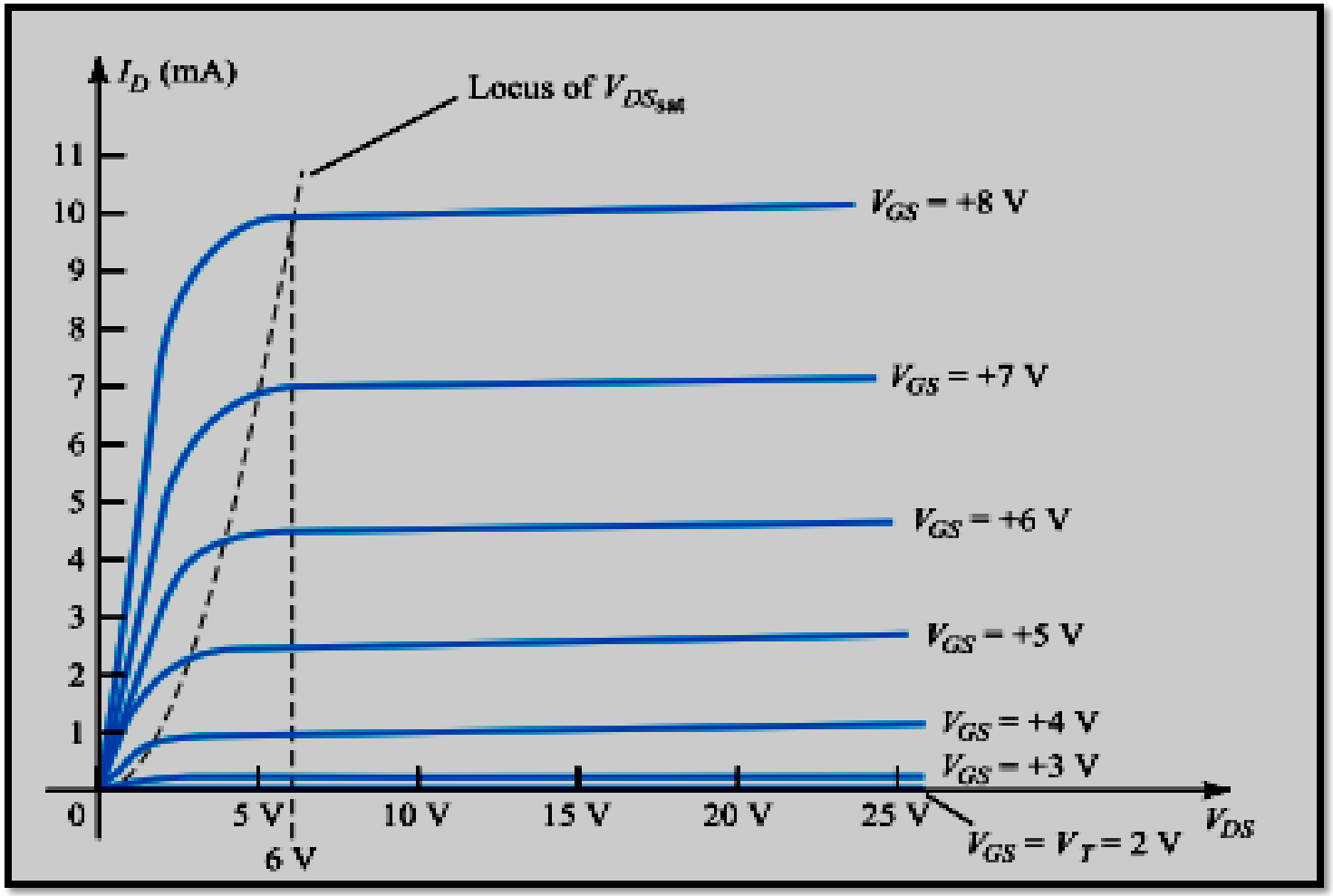
ii) Transfer characteristics:

It is the curve between drain current (I_D) and gate to source voltage (V_{GS}), while drain to source voltage (V_{DS}) should be constant.

Output Characteristics (Drain Characteristics)

- It is graph between output current I_D and output voltage V_{DS} at constant V_{GS}. It can be explained from working of the structure discussed above.
- For smaller values of V_{DS}, $I_D \propto V_{D.}$ So this region of the graph is called ohmic or linear region.
- In ohmic region the slope of the graph is dependent on V_{GS}. So MOSFET can be used as voltage controlled resistance.
- After pinch off condition the drain current become constant and this region of the graph is called saturation region.

Output Characteristics (Drain Characteristics)



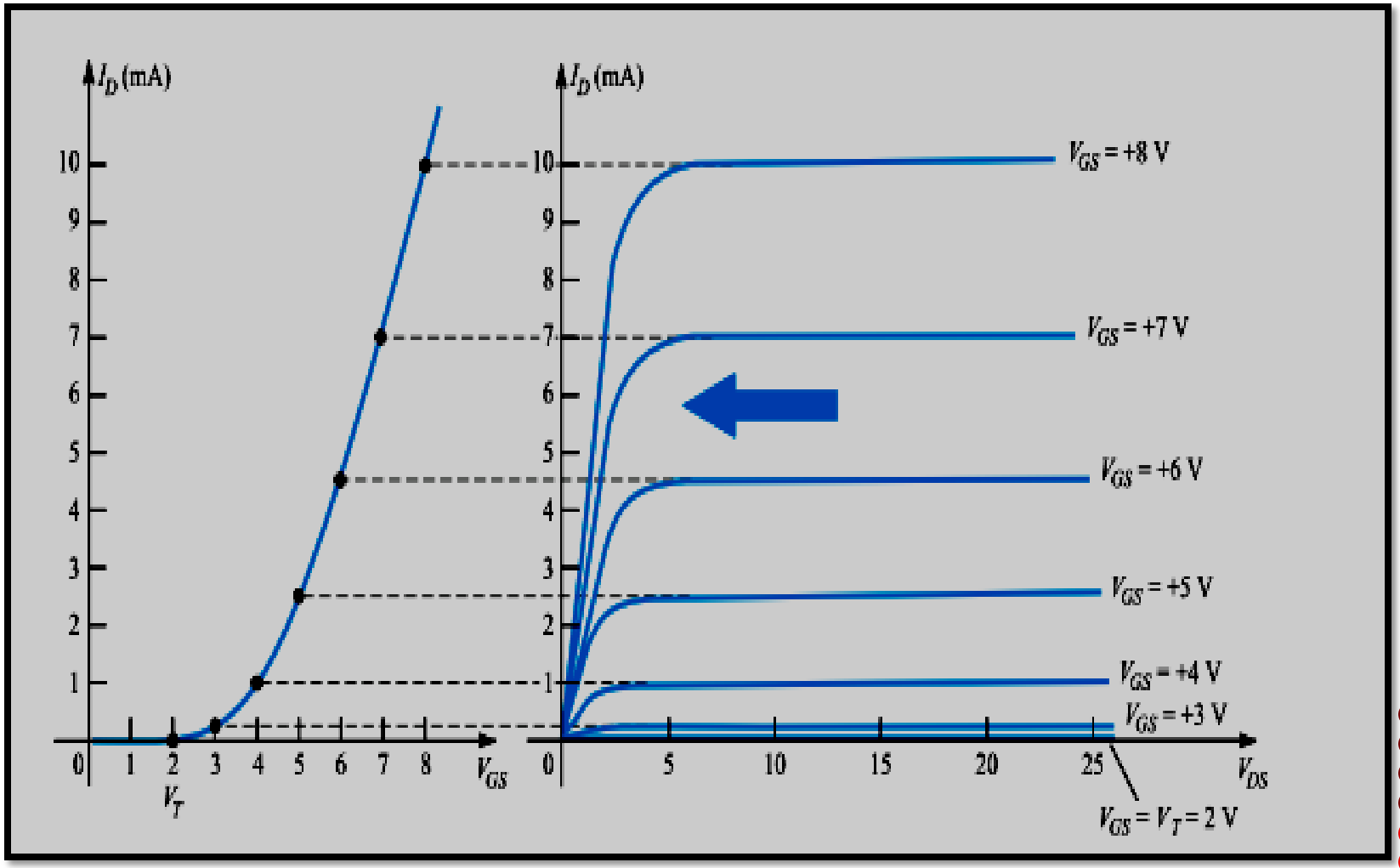
Transfer Characteristics

- It is graph between output current I_D and input voltage V_{GS}.
- The relation between I_D and V_{GS} can be given as:

$$\mathbf{I_D = k(V_{GS} - V_T)^2}$$

- Here k is a constant dependent on the construction of device
- The transfer curve can be obtained using above equation or from the output characteristics.
- Here V_T is called threshold voltage. It is minimum positive voltage required for n channel EMOSFET to start conduction through n channel.

Transfer Characteristics



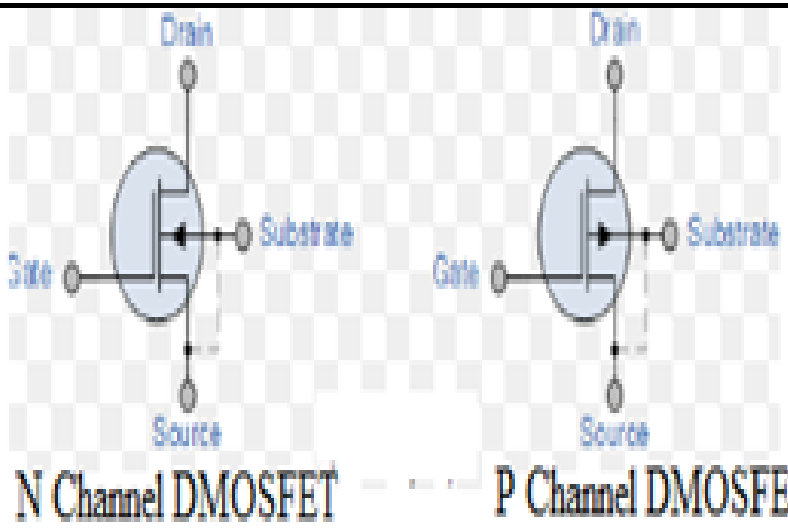
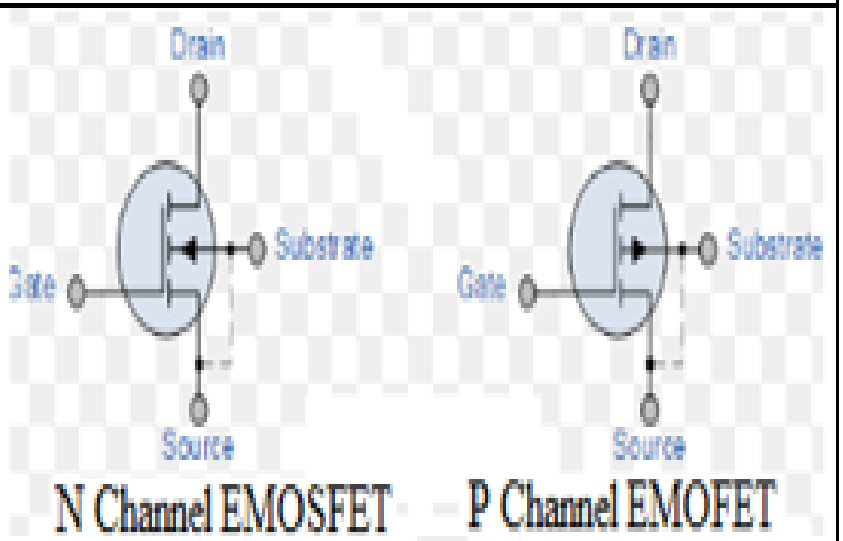
Transfer Characteristics

- Here two graphs are provided, with the vertical scaling in milliamperes for each graph. One is a plot of I_D versus V_{DS} , while the other is I_D versus V_{GS} .
- Using the drain characteristics on the right of the “y” axis, a horizontal line can be drawn from the saturation region of the curve denoted V_{GS} =0 V to the I_D axis. The resulting current level for both graphs is I_{DSS}.
- In a similar way for different values of V_{GS} we can note constant values of I_D from output curve.
- By joining all these points curve obtained is called transfer curve.

Difference Between BJT and FET(JFET, MOSFET)

S.N	BJT	JFET
1	It is bipolar device i.e. operation depends on majority and minority carrier both.	It is unipolar device i.e. operation depends only on majority carrier.
2	Current controlled device i.e. output is controlled by current.	Voltage controlled device i.e. output is controlled by voltage.
3	Input resistance is very low.	Input resistance is very high.
4	Temperature dependent due to minority carriers.	Temperature independent due to absence of minority carriers.
5	Power consumption is high.	Power consumption is low.
6	More noisy	Less noisy
7	Cost is low.	Cost is high

Comparison between EMOSFET & DMOSFET

S. No.	DMOSFET	EMOSFET
1		
2	Here channel is present between drain and source	Here channel is not present between drain and source
3	It operates for all values of V_{GS}	It operates only for $V_{GS} \geq V_t$ (for n channel)