Priyank Sharma (Electronics and Communication Engg.)

Soft Skills : Recently working on Cadence Virtuoso for Circuit Design.

Specialization

M.Tech: Communication Engineering

Ph.D: Low Power High Speed (VLSI field)

Area of Interest

Research Low Power High Speed (VLSI field)

Technology Development: ASLK Pro Kit designed & Sponsored by TI University program in Analog Domain, and also working on Cadence Virtuoso for Circuit Design.

Technology Transfer : ASLK Pro Kit- around 450 Students have been trained Under Texas CoE. (Lab Sponsored by TI University Progrmam)

Participated - In Specialized Training / Certified Courses: 3 FDP Organized as Program Coordinator Under Texas Instruments Center of Excellence, Dept. of Electronics & Communication Engineering. also Attended GIAN course & QIP short term course on Electronics and Communication Engineering.

Publication - Books / Chapters / Papers / Articles / Blogs • P. Sharma and S.Sharma, "Evaluation of Ultra-Low Power Techniques to 10T Junction Less Double Gate Hybrid Full Adder (10TJLDGHFA)," IEEE VLSI Circuits and System Letter,vol. 4 issue 4 ,Nov.2018.

• P. Sharma and S.Sharma,"Life Time of a MOS Degradation under Reliability Techniques (NBTI, HCI) in a Proposed 8T Full Adder" Journal of Nanoelectronics and Optoelectronics ,(Communicated 30-04-2019)

• Ravikant Saini and Priyank Sharma, "Study of PLC in Access Link & Indoor Channel," in Proc. 4th International Conference on Advanced Computing & Communication Technologies (ICACCT-2010), APIIT, Panipat, page196-199, 30 October, 2010.

• Priyank Sharma and M.P.Yadav, "Study of Different Coding Scheme in PLC System," in Proc. 2nd International Conference on Role of Tecnology in Nation Building (ICRTNB-2013), Subharti University, Meerut, page 300-303, 26-28 April, 2013.

Any other information

• Life member of Institute for Engineer and Research Publication (IFERP) Membership no. PMIN41569287
• Member of International Association of Engineers (IAENG) Membership no. 242131