Dr. Vikrant Varshney (Electronics and Communication)

Soft Skills: Self-Motivation, Leadership, Team-Work, Responsibility, Problem-Solving, Flexibility, Ability to Work Under Pressure and Time Management

Specialization

M.Tech: Microelectronics and VLSI Design

Ph.D: VLSI Design

Area of Interest

Research : Low Power VLSI Design; Analog/Mixed-Mode Signal Processing; Semiconductor Device Modelling; VLSI Circuits and Systems etc.

Technology Development: High-Speed, Low-Power and Low-Offset Comparators for Low-Voltage Ultra-Deep-Submicron ADC/DAC Applications

Participated - In Specialized Training / Certified Courses:

1. FDP on “Recent Trends in Photonics Technology” during 28 Dec. 2020 - 02 Jan. 2021 as Participant
2. FDP on "Design, Simulation & Measurement of Different Types of Antenna for 5G Applications Using HFSS" during 02-04 Nov. 2020 at MIET Meerut as an Organizer
3. SDIS-2020 during 27–31 Jan. ‘20 at REC Sonbhadra as Participant
4. AESM-2019 during 01–05 April ‘19 at MNNIT Allahabad as Participant
5. Faculty Orientation Programme during 19–20 July ‘18 at MNNIT Allahabad as Volunteer
6. 4th Research Evaluation Workshop-2018 during 13-15 Sep. ‘18 at MNIT Jaipur as Participant
7. Soft Skills (SS 2018) during 21–25 May ‘18 at MNNIT Allahabad as Volunteer and Participant
8. GIAN ANFE-2017 during 06–10 Nov. ‘17 at MNNIT Allahabad as Volunteer and Participant
9. CADIT-2017 during 22–27 Sep. ‘17 at MNNIT Allahabad as Volunteer and Participant
10. VDES-2017 during 14 June–15 July ‘17 at MNNIT Allahabad as Instructor
11. ADSPNIT-2017 during 27 Feb.–04 Mar. ‘17 at MNNIT Allahabad as Volunteer and Participant
12. VDES-2014 during 16 June–19 July ‘14 at MNNIT Allahabad as Instructor
13. MICROMOTS-2014 during 14–18 April ‘14 at MNNIT Allahabad as Participant

Publication - Books / Chapters / Papers / Articles / Blogs:

International Journals (SCI/SCIE/ESCI/SCOPUS):

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1. Vikrant Varshney, and Rajendra Kumar Nagaria. "Design and Analysis of Ultra High-Speed Low-Power Double Tail Dynamic Comparator using Charge Sharing Scheme." In: AEU-International Journal of Electronics and Communications 116, (2020): 153068:1-15. (SCIE) (IF: 2.853)

2. Vikrant Varshney, and Rajendra Kumar Nagaria. "An Unbalanced Clock Based Dynamic Comparator: A High-Speed Low-Offset Design Approach for ADC Applications." In: Advances in Electrical and Electronic Engineering 17, no. 4 (2019): 446-458. (ESCI and SCOPUS)

3. Vikrant Varshney, Avaneesh K. Dubey, and R. K. Nagaria. "Design and Performance of High-Speed Energy-Efficient CMOS Double Tail Dynamic Latch Comparator Using GACOBA Load Suitable for Low Voltage Applications." Journal of Circuits, Systems and Computers (2020). DOI: 10.1142/S0218126621501917 (SCIE) (IF: 1.363)

International Conferences:

1. Avaneesh K. Dubey, Vikrant Varshney, Ankur Kumar, Pratosh K. Pal, and R. K. Nagaria. "Low-Power Enhanced Speed Two-Tail Dynamically Controlled Comparator Suitable for Subthreshold CMOS Circuits." In: 2020 3rd International Conference on VLSI, Communication and Signal Processing (VCAS), MNNIT Allahabad, Oct. 2020. (Accepted) (SCOPUS Indexed)

2. Priyanka Singh, Vikrant Varshney, Ankur Kumar, and R. K. Nagaria. "DV-EXCCCII based Electronically Tunable Voltage Mode All Pass Filter." In: 2020 3rd International Conference on VLSI, Communication and Signal Processing (VCAS), MNNIT Allahabad, Oct. 2020. (Accepted) (SCOPUS Indexed)

3. Ankur Kumar, Avaneesh K. Dubey, Vikrant Varshney, Priyanka Singh, and R. K. Nagaria. "A hybrid technique to minimize the leakage of wide Fan-in OR-logic Domino Circuit." In: 2020 3rd International Conference on VLSI, Communication and Signal Processing (VCAS), MNNIT Allahabad, Oct. 2020. (Accepted) (SCOPUS Indexed)

4. Priyanka Singh, Vikrant Varshney, Ankur Kumar, and R. K. Nagaria. "DV-EXCCCII based Electronically Tunable Current mode filter." In: 2020 3rd International Conference on VLSI, Communication and Signal Processing (VCAS), MNNIT Allahabad, Oct. 2020. (Accepted) (SCOPUS Indexed)

5. Abhinav Gupta, Vikrant Varshney, Adarsh Vishwakarma, Arunabh Kishore, Atul Pal, Piyush Mishra, Varnika Pathak, and Ziyaur Rahman. "A Comparative Investigation of SiGe Junctionless Triple Gate (JLTG) and Junctionless Gate-All-Around (JL-GAA) MOSFET." In: 2020 3rd International Conference on VLSI, Communication and Signal Processing (VCAS), MNNIT Allahabad, Oct. 2020. (Accepted) (SCOPUS Indexed)

6. Himanshi Awasthi, Nitish Kumar, Vaibhav Purwar, Abhinav Gupta, Vikrant Varshney, and Sanjeev Rai. "Comparative Study of Silicon and In0:53Ga0:47As-Based Gate-All-Around (GAA) MOSFETs." In: 2020 3rd International Conference on VLSI, Communication and Signal Processing (VCAS), MNNIT Allahabad, Oct. 2020. (Accepted) (SCOPUS Indexed)

7. Keshav K. Mishra, Avaneesh K. Dubey, Vikrant Varshney, and Kamal Prakash Pandey. "Energy Efficient 16T Hybrid-CMOS Full Adder using Novel Full Swing XNOR Logic." In: 2020 6th IEEE Students' Conference on Engineering & Systems (SCES), MNNIT Allahabad, pp. 1-6, IEEE, July 2020.

8. Priyanka Singh, Vikrant Varshney, Ankur Kumar, and R. K. Nagaria. "Electronically Tunable First Order Universal Filter based on CCDDCCTA." In: 2019 3rd IEEE International Conference on Information and Communication Technology (CICT), Allahabad, pp. 1-6, IEEE, Dec. 2019. (SCOPUS Indexed)

9. Avaneesh K. Dubey, Pratosh K. Pal, Vikrant Varshney, Ankur Kumar, and R. K. Nagaria. "Impact of Channel Doping Fluctuation and Metal Gate Work Function Variation in FD-SOI MOSFET for 5nm BOX Thickness." In: 2019 3rd IEEE International Conference on Information and Communication Technology (CICT), Allahabad, pp. 1-4, IEEE, Dec. 2019. (SCOPUS Indexed)

10. Vikrant Varshney, Ankur Kumar, Avaneesh K. Dubey, Priyanka Singh, and R. K. Nagaria. "A High-Speed Energy-Efficient CMOS Dynamic Latch Comparator for Low-Voltage Applications." In: 2019 6th IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics (UPCON), Aligarh, pp. 1-6, IEEE, Nov. 2019. (SCOPUS Indexed)

11. Ankur Kumar, Vikrant Varshney, Priyanka Singh, and R. K. Nagaria. "A Variation and Noise Tolerant Wide Fan-in OR-Logic Domino Circuit." In: 2019 6th IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics (UPCON), Aligarh, pp. 1-6, IEEE, Nov. 2019. (SCOPUS Indexed)

12. Avaneesh K. Dubey, Pratosh K. Pal, Vikrant Varshney, Ankur Kumar, and R. K. Nagaria. "Design and Performance of High-Speed Low-Offset CMOS Double-Tail Dynamic Comparators using Offset Control Scheme." In: 2019 9th IEEE Annual International Conference on Information Technology, Electromechanical and Microelectronics (IEMECON), Jaipur, pp. 49-55, IEEE, Mar. 2019. (SCOPUS Indexed)

13. Ankur Kumar, Vikrant Varshney, Pratosh K. Pal, Avaneesh K. Dubey, and R. K. Nagaria "A Modified High Speed Domino with Low Leakage for Wide Fan-in Domino OR-Gate" In: 2018 14th IEEE Uttar Pradesh Section International Conference on Computer, Electrical and Electronics (INDICON), Coimbatore, pp. 1-6, IEEE, Dec. 2018. (SCOPUS Indexed)

14. Pratosh K. Pal, Avaneesh K. Dubey, Ankur Kumar, Vikrant Varshney, and R. K. Nagaria. "A 0.55V, 28.6ppm/oC Nanopower Subthreshold Voltage Reference with Body Biasing." In: 2018 14th IEEE Uttar Pradesh Section International Conference on Computer, Electrical and Electronics (INDICON), Coimbatore, pp. 1-6, IEEE, Dec. 2018. (SCOPUS Indexed)

15. Vikrant Varshney, Avaneesh K. Dubey, Ankur Kumar, Pratosh K. Pal, and R. K. Nagaria. "Design of Power Efficient Low-Offset Dynamic Latch Comparator using 90nm CMOS Process." In: 2018 3rd International Conference on Innovative Applications of Computational Intelligence on Power, Energy and Controls with their Impact on Humanity (CIPECH), Ghaziabad, pp. 229-233, IEEE, Nov. 2018. (SCOPUS Indexed)

16. Rahul Jain, Avaneesh K. Dubey, Vikrant Varshney, and Rajendra K. Nagaria. "Design of low-power high-speed double-tail dynamic CMOS comparator using novel latch structure." In: 2017 4th IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics (UPCON), Mathura, pp. 217-222, IEEE, Oct. 2017. (SCOPUS Indexed)

Book Chapters:

1. Avaneesh K. Dubey, Vikrant Varshney, Ankur Kumar, Pratosh K. Pal, and R. K. Nagaria. "Design and performance of High-Speed CMOS Double tail Dynamic Comparator suitable for Mixed-Signal ICs." In Advances in VLSI, Communication, and Signal Processing, Springer, Singapore, 2020. ISBN: 978-981-15-6839-8 (SCOPUS Indexed)

2. Ankur Kumar, Pratosh K. Pal, Vikrant Varshney, Avaneesh K. Dubey, and R. K. Nagaria. "Leakage Tolerant Low Power Wide Fan-in OR-Logic Domino Circuit." In Advances in VLSI, Communication, and Signal Processing, Springer, Singapore, 2020. ISBN: 978-981-15-6839-8 (SCOPUS Indexed)