UNIT-1 COMPUTER ORGANIZATION AND ARCHITECTURE(KCS-302)

ASSIGNMENT NO.1

Q 1: Represent the following conditional control statements by two register transfer statements with control functions:
If(P=1) then (R1<-R2) else if(Q=1) then(R1<--R3).

Q 2: The following transfer statements specify a memory operation.Explain the memory operation in each case.
(i) R2 <--M[AR]
(ii) M[AR] <--R3,
(iii) R5 <--M[R5]

Q 3: Let SP=000000 in the stack.How many items are there in stack if:
a)FULL=1 and EMPTY=0?
b)FULL=O and EMPTY=1?

Q5: A General register organization has 16 register with 32 bits in each ALU and a destination decoder.
(i)How many multiplexers are there in the A bus and what is the size of each multiplexer?
(ii)How many selection inputs are needed for MUX A and MUX B?
(iii)How many inputs and outputs are there in the decoder?
(iv)Formulate a control word for the system assuming that the ALU has 35 operations.

Q6: An instruction is stored at location 300 with its address field at location 301.The address field has the value 400.A processor registers Rl contains the number 200.Evaluate the effective address if the addressing mode of the instruction is(a)direct;(b)immediate;(c)relative;(d)register indirect;(e)index with R,as the index register.

UNIT-2 COMPUTER ORGANIZATION AND ARCHITECTURE(RCS-302)

ASSIGNMENT NO.2

Q.1 Discuss the required hardware,algorithm for Booth's Multiplication Algorithm.Iterate your algorithm for the product(+13)*(-19)**.**

Q.2 Differentiate between hard wired and micro program control.

Q.3 What is zero address instruction?Explain with the help of an example.

Q.4 Represent(-307.1875) in IEEE standard format using single precision and double precision format.

Q.5 What do you mean by instruction cycle?

Q.6 Design a 4 bit array multiplier.
Q.7 Design a 4 bit adder and subtractor circuits.

Q.8 Perform the division operation on19/2 using restoring division method.

Q.9 Desing a hardware diagram and flow chart of boot multiplication.

Q.10 Perform the operation on (-12)*(12) sign-multiplication method .

UNIT-3 COMPUTER ORGANIZATION AND ARCHITECTURE RCS302

Assignment-3

Q.1 Define instruction pipeline.Explain four segment pipelines with help of flowchart,
Q.2 Differentiate between Horizontal and vertical micro programming.Suppose there are 136 control signals in a processor data path.Calculate control word size for horizontal&vertical encoding.

Q.3 Explain attached array and SIMD array processor.

Q.4 What is throughput?Discuss Flynn's classification in brief.

Q.5 How pipeline performance can be measured?Discuss.Give a space time diagram for visualizing the pipeline behavior for a four stage pipeline.
Q.6 Write the control sequence for the micro operation MOVE R2,#20(R2=20).
Q.7 Expalin hardwired and micro-programmed control Unit with neat and clean diagram.

Q.8 Write the control sequence of execution of complete instruction SUB (R1),R2.

Q 9: What do you mean by micro-program sequencing? Explain Microinstruction with next address field.
Q.10 Write a program to evaluate the arithmetic statements:
X=(A-B+C*(D*E-F))/(G+H*K)
a.Using general register computer with 3-address instruction.
b.Using general register computer with 2-address instruction.
C.Using an accumulator type computer with 1-address instruction.
d.Using stack organized computer with O-address instruction

UNIT-4 [COMPUTER ORGANIZATION AND ARCHITECTURE(RCS-302)]

Assignment No. 4

Q.1 What is a mapping function?What are the ways the cache can be mapped?Explain in detail.
a.Discuss pipeline conflicts and their solutions.
Q.2 Explain the Address Translation in Virtual Memory.
Q.3 A digital computer has a memory unit of 64K x 16 and a cache memory of 1K words.The cache uses direct mapping with a block size of four words.
a.How many bits are there in the tag,index,block,and word fields of the address format?
b.How many bits are there in each word of cache,and how are they divided into functions?Include a valid bit.
c.How many blocks can the cache accommodate?
Q.4 An address space is specified by 24 bits and the corresponding memory space by 16 bits.
a.How many words are there in the address space?
b.How many words are there in the memory space?
c.If a page consists of 2K words,how many pages and blocks are there in the system?
Q.5 The logical address space in a computer system consists of 128 segments.Each segment can have up to
32 pages of 4K words in each.Physical memory consists of 4K blocks of 4K words in each.Formulate the logical and physical address formats
Q.6 Explain magnetic disk,magnetic tape and optical disks in detail.
Q.7 What do you mean by virtual memory explain in detail.
Q.8 Define Memory. Write in detail about memory hierarchy.

UNIT-5 COMPUTER ORGANIZATION AND ARCHITECTURE(RCS-302)

Assignment No.5

Q.1 What do you mean by vector and non-vector interrupt.
Q.2 What is I/O port.
Q.3 What is the difference between Isolated I/O and memory-mapped I/O?Wi
at are advantage and disadvantage of each?
Q.4 Differentiate between
a)Parallel and serial data transfer
b)Synchronous and asynchronous data transfer
Q.5 What is DMA?Explain DMA controller in detail.
Q.6 What is mode of transfer?Explain the difference between programmed I/O and interrupt initiated I/O.
Q7.Discuss the working principal of I/O processors(IOP).Explain the process of communication between CPU and IOP.