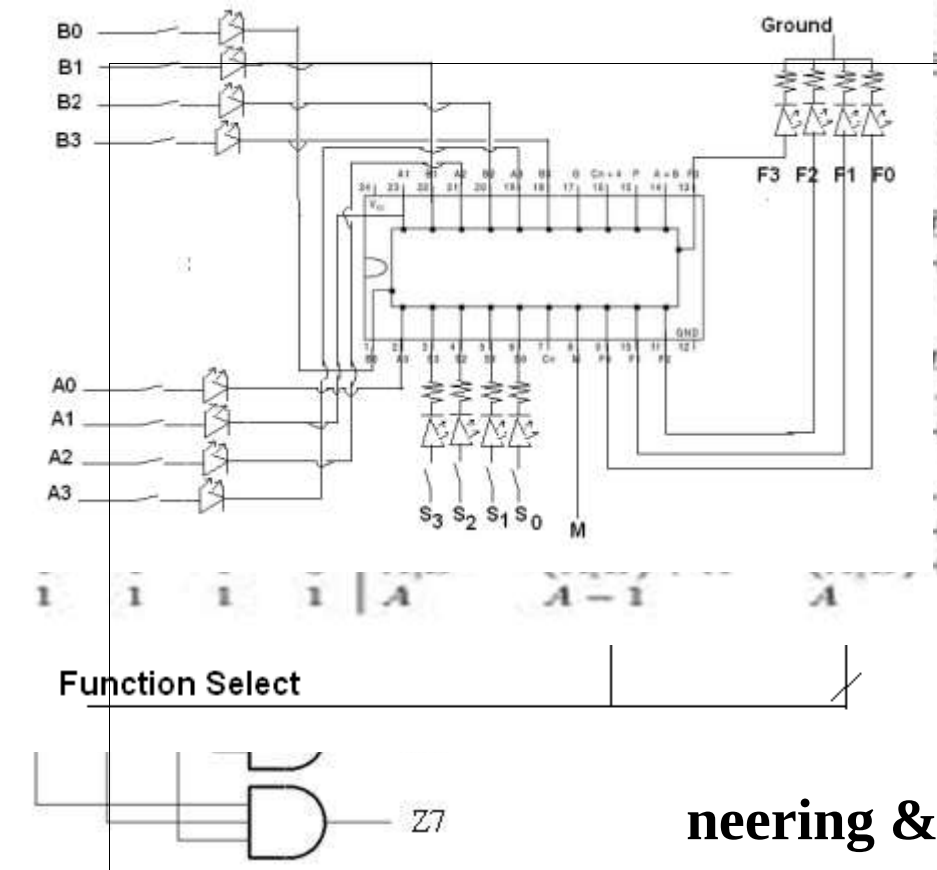


Meerut Institute of Engineering & Technology

Department of Computer Science & Engineering

DR. A.P.J KALAM TECHNICAL UNIVERSITY
LUCKNOW

LAB MANUAL

B.TECH
COMPUTER SCIENCE AND ENGINEERING
SESSION – 2018-2019

Lab Code: RCS-352
COMPUTER ORGANIZATION LAB

Faculty Name:

Mr. Sanjay Sonkar
(Assistant Professor)

Index

List of Lab Outcomes

LO1: To realize the adder circuits using basic gates.
LO2: To realize the converter circuits using basic gates.
LO3: To learn and understand the working of Multiplexer by using IC 74153
LO4: To learn about working principle of decoder by using IC 74LS139
LO5: To understand the circuits for ALU,

MEERUT INSTITUTE OF ENGINEERING & TECHNOLOGY, MEERUT
N.H. 58, Delhi-Roorkee Highway, Baghpat Road Bypass Crossing, Meerut-250005

List of Program

1. Implementing HALF ADDER, FULL ADDER using basic logic gates.
2. Implementing Binary -to –Gray and Gray -to -Binary code conversions.
3. Implementing 3-8 line DECODER.
4. Implementing 4x1 and 8x1 MULTIPLEXERS.
5. Verify the Truth Table of *SR* FLIP-FLOPS.
6. Verify the Truth Table of *D* FLIP-FLOPS.
7. Verify the Truth Table of *JK* FLIP-FLOPS.
8. Verify the Truth Table of *T* FLIP-FLOPS.
9. Implementing HALF SUBTRACTOR, FULL SUBTRACTOR using basic logic gates.
10. Design of an 4-bit ARITHMETIC LOGIC UNIT.

VALUE ADDITION:

1. Design the data path of a computer from its register transfer language description.
2. Design the control unit of a computer using either hardwiring or microprogramming based on its register transfer language description.
3. Implement a simple instruction set computer with a control unit and a data path.

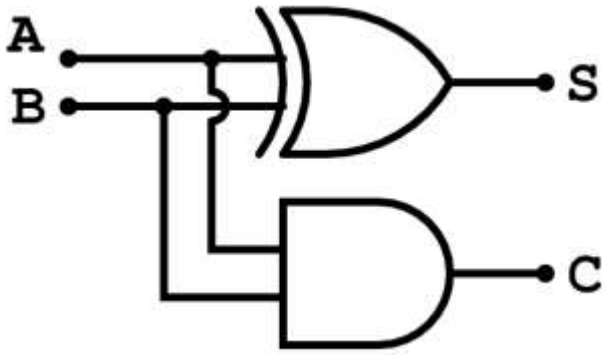
MEERUT INSTITUTE OF ENGINEERING & TECHNOLOGY, MEERUT
N.H. 58, Delhi-Roorkee Highway, Baghpat Road Bypass Crossing, Meerut-250005

Experiment No.-1

Objective: Implementing HALF ADDER, FULL ADDER using basic logic gates

Half adder: A half adder is a logical circuit that performs an additional operation on two binary digits. The half adder produces a sum and a carry value, which are both binary digits.

A half adder circuit has two inputs A and B and two outputs – S representing sum and C representing carry.



S = A XOR B i.e. (A'B + AB')

C = A AND B i.e. (A.B)

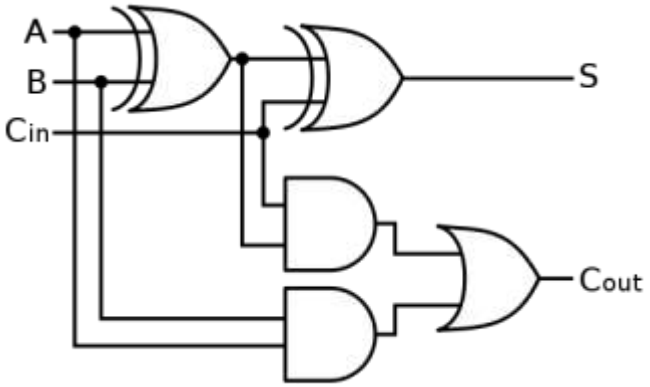
TRUTH TABLE:

A	B	S	C
0	0	0	0

0	1	1	0
1	0	1	0
1	1	0	1

Full Adder: A full adder is a logical circuit that performs an additional operation on three binary digits. The half adder produces a sum and a carry value which are both binary digits.

A full adder circuit has three inputs *A, B* and C_{in} and two outputs – S representing sum and C_{out} representing carry.



S = A xor B xor C

C = A.B +C(A xor B)

TRUTH TABLE:

A	**B**	**Cin**	**S**	**Cout**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1

1	1	0	0	1
1	1	1	1	1

PROCEDURE:-

1. Make the connections
2. Apply the voltage
3. Verify the table

RESULT: - . Truth table of half adder and full adder has verified.

PRECAUTIONS:-

1. All Connections should be according to circuit diagram.
2. All Connections should be right and tight.
3. Reading should be taken carefully.
4. Switch off Power supply after completing the Experiment

MEERUT INSTITUTE OF ENGINEERING & TECHNOLOGY, MEERUT
N.H. 58, Delhi-Roorkee Highway, Baghpat Road Bypass Crossing, Meerut-250005

Experiment No.-2

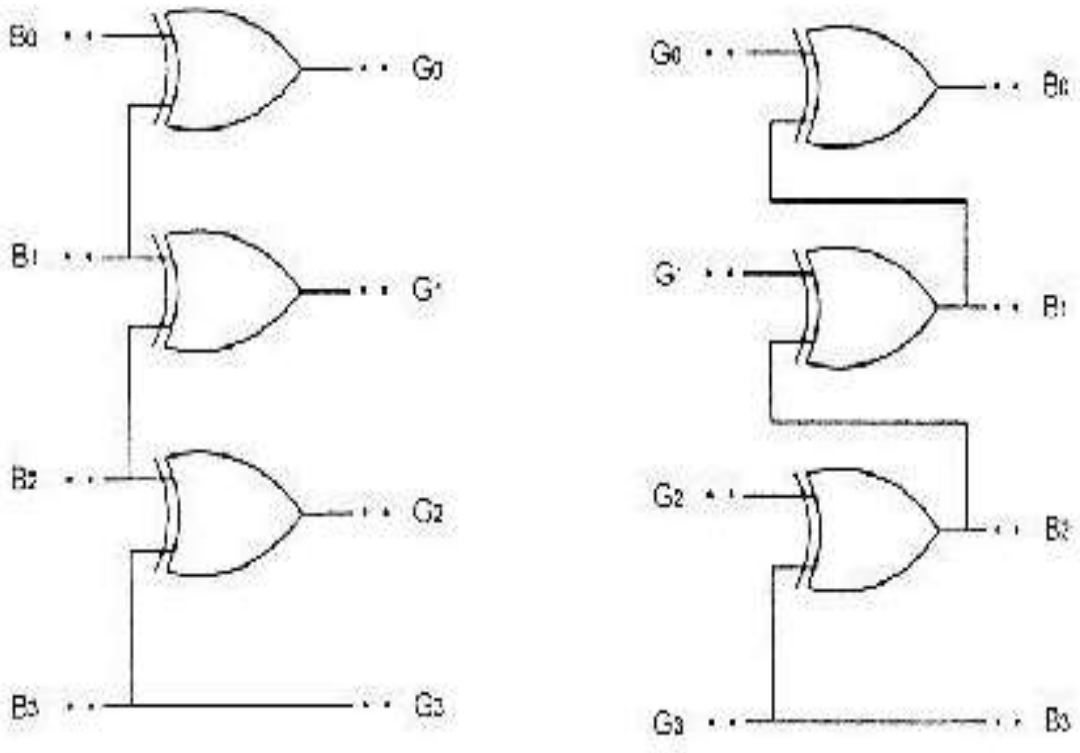
Objective:
Implementing Binary -to –Gray and Gray -to -Binary code conversions.

.
APPARATUS REQUIRED: - Bread Board, ICs- 7486, Connecting wire,Power supply etc.

THEORY:- The gray code is a non-weighted code. The successive gray code differs in one bit position only that means it is a unit distance code. It is also referred as cyclic code. Binary code is the simplest form of computer code or programming data. It is represented entirely by a binary system of digits consisting of a string of consecutive zeros and ones.

Logic diagram & Truth Table:

(Logic 1 = +5V & Logic 0= GND)



Decimal	B3	B2	B1	B0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Binary code
Table 1

Decimal	G3	G2	G1	G0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	0	1	0
4	0	1	1	0
5	0	1	1	1
6	0	1	0	1
7	0	1	0	0
8	1	1	0	0
9	1	1	0	1
10	1	1	1	1
11	1	1	1	0
12	1	0	1	0
13	1	0	1	1
14	1	0	0	1
15	1	0	0	0

Gray code
Table 2

Procedure:

1. Connect +5 V and ground to their indicated position on DB06 experiment board from external DC power supply.
2. Connect inputs B0, B1, B2, B3 as per truth table 2 to binary to gray code converter as shown in figure
3. Switch ON the power supply.
4. Observe output G0, G1, G2, G3 on multi-meter or on LED Display
5. Repeat above step for remaining inputs and prove truth table.
6. Repeat above steps for gray to binary code converter and prove truth table

Result: The observation of conversion is verified.

Precautions:

1. All connection should be according to circuit diagram.
2. All connections should be right and tight.
3. Switch off power supply when done.

MEERUT INSTITUTE OF ENGINEERING & TECHNOLOGY, MEERUT
N.H. 58, Delhi-Roorkee Highway, Baghpat Road Bypass Crossing, Meerut-250005

Program No.-3

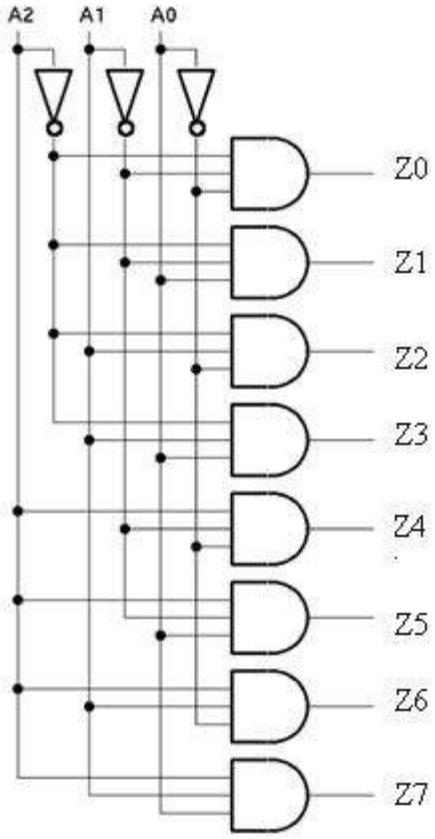
Objective:
Implementing 3-8 line DECODER.

APPARATUS REQUIRED - Bread Board, ICs- 74138, connecting wire etc.

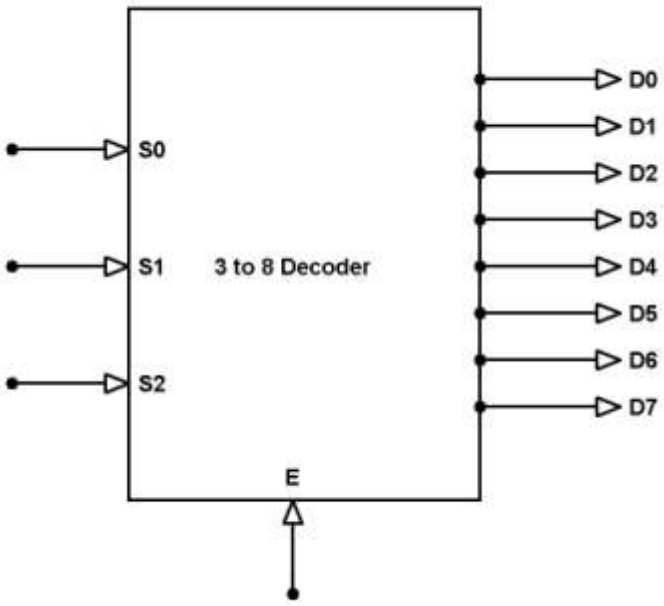
THEORY:

Decoder
A decoder is a combinational logic circuit , which is used to change the code into a set of signals. It is the reverse process of an encoder. A decoder circuit takes multiple inputs and gives multiple outputs. A decoder circuit takes binary data of 'n' inputs into '2^n' unique output. In addition to input pins, the decoder has a enable pin. This enables the pin when negated, makes the circuit inactive

Circuit Diagram:



Pin Diagram:



Truth Table:

S0	S1	S2	E	D0	D1	D2	D3	D4	D5	D6	D7
x	x	x	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	1	0	0	0	0	0	0	1	0
0	1	0	1	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	1	0	0	0
1	0	0	1	0	0	0	1	0	0	0	0
1	0	1	1	0	0	1	0	0	0	0	0
1	1	0	1	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

1) Connect +5 V and ground to their indicated position
2) Make all connection according to the diagram
3) Switch ON the power supply.
4) Check the output according to table
5) Repeat above step for remaining inputs and prove truth table.

Result: The truth table of 3:8 Decoder is verified.

Precautions:

4. All connection should be according to circuit diagram.
5. All connections should be right and tight.
6. Switch off power supply when done.

MEERUT INSTITUTE OF ENGINEERING & TECHNOLOGY, MEERUT
N.H. 58, Delhi-Roorkee Highway, Baghpat Road Bypass Crossing, Meerut-250005

Program No.-4

Objective:
Implementing 4x1 and 8x1 MULTIPLEXERS.

APPARATUS REQUIRED - Bread Board, ICs- 74151A (8×1 MUX), connecting wire etc.

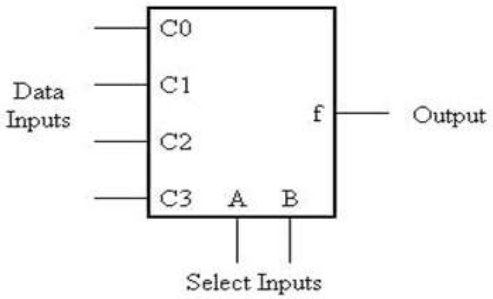
THEORY:

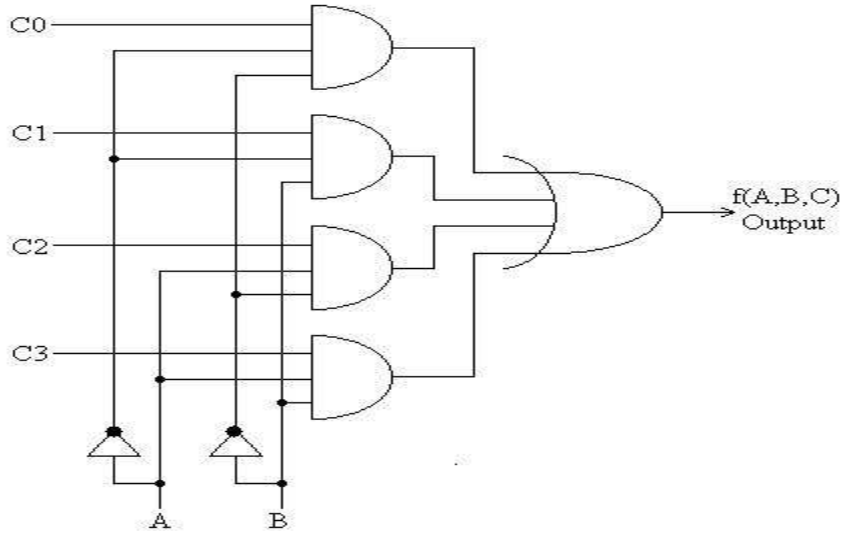
Multiplexer: A multiplexer is a device that performs multiplexing i.e. it selects one of many analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has *n* select lines, which are used to select which input line to be sent to the output.

4:1 MULTIPLEXER: It consists of 4 inputs, 2 selection line and 1 outputs

Truth Table

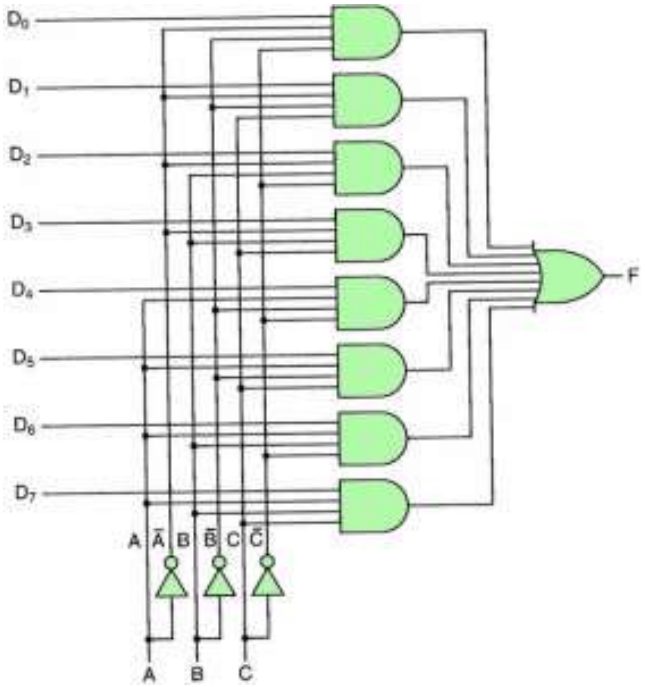
Selection Input		Output
A	**B**	**f**
0	**0**	**C0**
0	**1**	**C1**
1	**0**	**C2**
1	**1**	**C3**





8:1 Multiplexer: It consist of 8 inputs, 3 selection lines and 1 output. The 8-to-1 multiplexer requires 8 AND gates, one OR gate and 3 selection lines. As an input, the combination of selection inputs are giving to the AND gate with the corresponding input data lines.

A	B	C	F
0	0	0	D0
0	0	1	D1
0	1	0	D2
0	1	1	D3
1	0	0	D4
1	0	1	D5
1	1	0	D6
1	1	1	D7



Procedure:

6) Connect +5 V and ground to their indicated position
7) Make all connection according to the diagram
8) Switch ON the power supply.
9) Check the output according to table
10) Repeat above step for remaining inputs and prove truth table.

Result: The truth table of 4:1 MUX and 8:1 MUX is verified.

Precautions:

7. All connection should be according to circuit diagram.
8. All connections should be right and tight.
9. Switch off power supply when done.

MEERUT INSTITUTE OF ENGINEERING & TECHNOLOGY, MEERUT
N.H. 58, Delhi-Roorkee Highway, Baghpat Road Bypass Crossing, Meerut-250005

Experiment No.-5

Objective:
Verify the truth tables of *SR* FLIP-FLOPS.

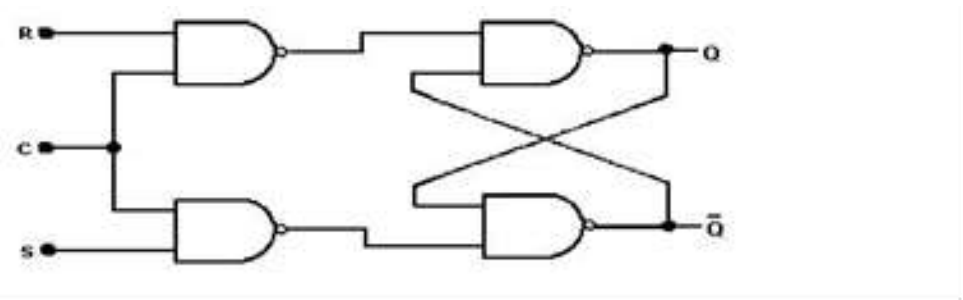
APPARATUS REQUIRED: - Digital Trainer Kit, ICs, (7400, 7404, 7410) & Connecting wire.

THEORY: - A Flip flop is a bi-stable electronic circuit that has two stable state .That is , its output is either +5V(logic 1) or 0V(logic 0) .A Flip Flop can be referred as memory device since its output will remain unchanged until its input is not changed. It is used to store one binary digit.

S-R FLIP FLOP:- A R-S Flip Flop is one that has two inputs R & S and two outputs Q & Q'. An R-S Flip Flop can be constructed using NOR gates or NAND gates. Figure shows R-S Flip Flop constructed using four NAND gates.

CIRCUIT DIAGRAM:-

.



Truth table:

CLK	S	R	Q(t+1)
0	**x**	**x**	**No Change**
1	**0**	**0**	**No Change**
1	**0**	**1**	**Reset**
1	**1**	**0**	**Set**
1	**1**	**1**	**No Change**

Procedure:

1) Connect +5 V and ground to their indicated position
2) Make all connection according to the diagram
3) Switch ON the power supply.
4) Check the output according to table
5) Repeat above step for remaining inputs and prove truth table.

Result: The Truth table of *SR* flip-flop has verified.

Precautions:

10. All connection should be according to circuit diagram.
11. All connections should be right and tight.
12. Switch off power supply when done.

MEERUT INSTITUTE OF ENGINEERING & TECHNOLOGY, MEERUT
N.H. 58, Delhi-Roorkee Highway, Baghpat Road Bypass Crossing, Meerut-250005

Experiment No.-6

Objective:
Verify the truth tables of *D* FLIP-FLOPS.

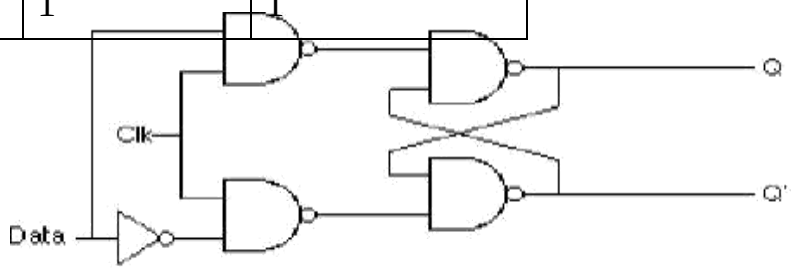
APPARATUS REQUIRED: - Digital Trainer Kit, ICs, (7400, 7404, 7410) & Connecting wire.

THEORY: -

D- FLIP FLOP: - To avoid the forbidden case that occur in R-S Flip Flop, when R=S=1, D Flip Flop is implemented. In the D Flip Flop, there is only one input D as show in figure .We can transmit the value of D at the output of the Flip Flop when CLK is high.

Truth Table

CLK	D	Q(t+1)
0	X	No Change
1	0	0
1	1	1



Procedure:

6) Connect +5 V and ground to their indicated position
7) Make all connection according to the diagram
8) Switch ON the power supply.
9) Check the output according to table
10) Repeat above step for remaining inputs and prove truth table.

Result: The Truth table of *D* flip-flop has verified.

Precautions:

1. All connection should be according to circuit diagram.
2. All connections should be right and tight.
3. Switch off power supply when done.

MEERUT INSTITUTE OF ENGINEERING & TECHNOLOGY, MEERUT
N.H. 58, Delhi-Roorkee Highway, Baghpat Road Bypass Crossing, Meerut-250005

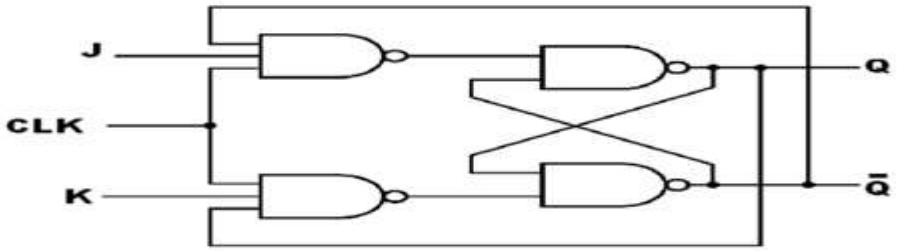
Experiment No.-7

Objective:
Verify the truth tables of *JK* FLIP-FLOPS.

APPARATUS REQUIRED - Digital Trainer Kit, ICs, (7400, 7404, 7410) & Connecting wire.

THEORY: -

J-K FLIP FLOP: - Setting R=S=1 with a R-S Flip Flop Q and Q' will set to the same logic level. J-K Flip Flop accounts for this illegal input this illegal conditions .The. It is used to build counter. The values of J and K determine what a J-K Flip Flop does on the next clock edge. When both are low, the Flip Flop retains its last state. When J is low and K is high, the Flip Flop resets. When J is high and K is low, the Flip Flop sets. When both are high, the Flip-flop toggles. In this last mode, the J-K Flip Flop can be used as a frequency divider.



Truth table:

CLK	J	K	Q(t+1)
0	x	x	No Change
1	0	0	No Change
1	0	1	Reset
1	1	0	Set
1	1	1	Toggle

Procedure:

11) Connect +5 V and ground to their indicated position

12) Make all connection according to the diagram

13) Switch ON the power supply.

14) Check the output according to table

15) Repeat above step for remaining inputs and prove truth table.

Result: The Truth table of *JK* flip-flop has verified.

Precautions:

4. All connection should be according to circuit diagram.
5. All connections should be right and tight.
6. Switch off power supply when done.

Experiment No.-8

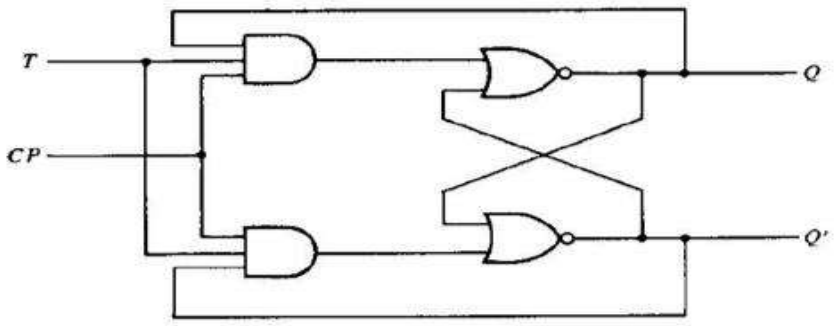
Objective:

Verify the truth tables of *T* FLIP-FLOPS.

APPARATUS REQUIRED: - Digital Trainer Kit, ICs, (7400, 7404, 7410) & Connecting wire.

THEORY: -

T-Flip-flop: The T- Flip Flop is known as Toggle Flip flop. The T Flip flop is a modification of the JK Flip flop by connecting both inputs J and K together. Figure shows the logic diagram of T flip-flop, logic symbol and truth table of T Flip flop is also shown. When T=0, both AND gates are disabled and hence there is no change in the previous output. When T=1 (J=K=1) output toggles. Toggles means that the output is 0 when the previous state is 1 otherwise output is 1 when the previous state is 0. Therefore, the output is a complement of the previous output.



Truth Table

T	Q(t)	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Procedure:

1) Connect +5 V and ground to their indicated position
2) Make all connection according to the diagram
3) Switch ON the power supply.
4) Check the output according to table

5) Repeat above step for remaining inputs and prove truth table.

Result: The Truth table of *T* flip-flop has verified.

Precautions:

1. All connection should be according to circuit diagram.
2. All connections should be right and tight.
3. Switch off power supply when done.

Experiment No.-9

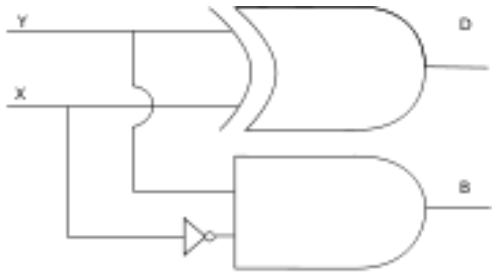
Objective:

Implementing HALF SUBTRACTOR, FULL SUBTRACTOR using basic logic gates.

APPARATUS REQUIRED - Digital Trainer Kit, ICs, (7400, 7404, 7410) & Connecting wire.

THEORY:

Half Subtractor: A half-subtractor is a logical circuit that performs a subtraction operation on two binary digits. The half subtractor produces a Difference and a borrow value which are both binary digits. A half-subtractor circuit has two inputs X, Y and two outputs – D representing difference and B representing borrow.



D = A XOR B i.e. (A'B + AB')

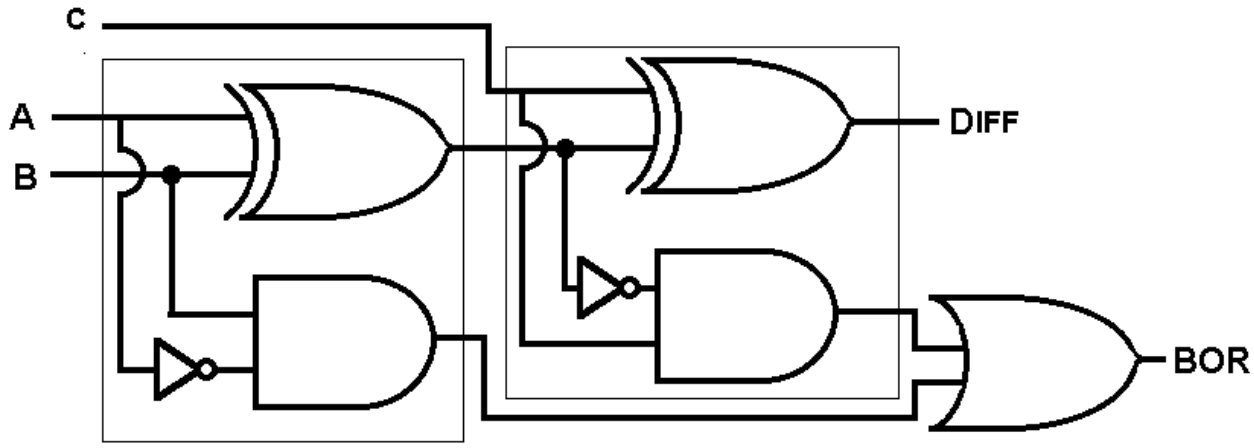
B = A'B

TRUTH TABLE:

X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Full Subtractor: A full-subtractor is a logical circuit that performs a subtraction operation on three binary digits. The full-subtractor produces a difference and a borrow value which are both binary digits.

A Full adder circuit has three inputs A, B and C and two outputs – DIFF representing difference and BOR representing borrow.



S = A xor B xor C

C = A'.B +C(A xnor B)

TRUTH TABLE:

A	B	C	DIFF	BOR
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Procedure:

1) Connect +5 V and ground to their indicated position
2) Make all connection according to the diagram
3) Switch ON the power supply.
4) Check the output according to table
5) Repeat above step for remaining inputs and prove truth table.

Result: The Truth table of *Half-Subtractor and full-Subtractor* has verified.

Precautions:

1. All connection should be according to circuit diagram.
2. All connections should be right and tight.
3. Switch off power supply when done.

MEERUT INSTITUTE OF ENGINEERING & TECHNOLOGY, MEERUT
N.H. 58, Delhi-Roorkee Highway, Baghpat Road Bypass Crossing, Meerut-250005

Experiment No.-10

OBJECTIVE: Design of a 4-bit Arithmetic Logic Unit.

APPARATUS REQUIRED IC 74181 LEDs, Power Supply, CRO, Multimeter

THEORY:

ALU stands for the arithmetic and logical unit and is one of the important unit in almost all the calculating machine these days be it with the hand-held mobile, or computers. This unit carries out all the computational work in the system. The typical ALU sizes are:
4-bit ALU: ALU that processes two 4-bit numbers.
8-bit ALU: ALU that processes two 8-bit numbers.

Still in the latest systems ALU sizes are 16, 32, 64-bit etc.

Following figure shows the block diagram of a typical ALU.

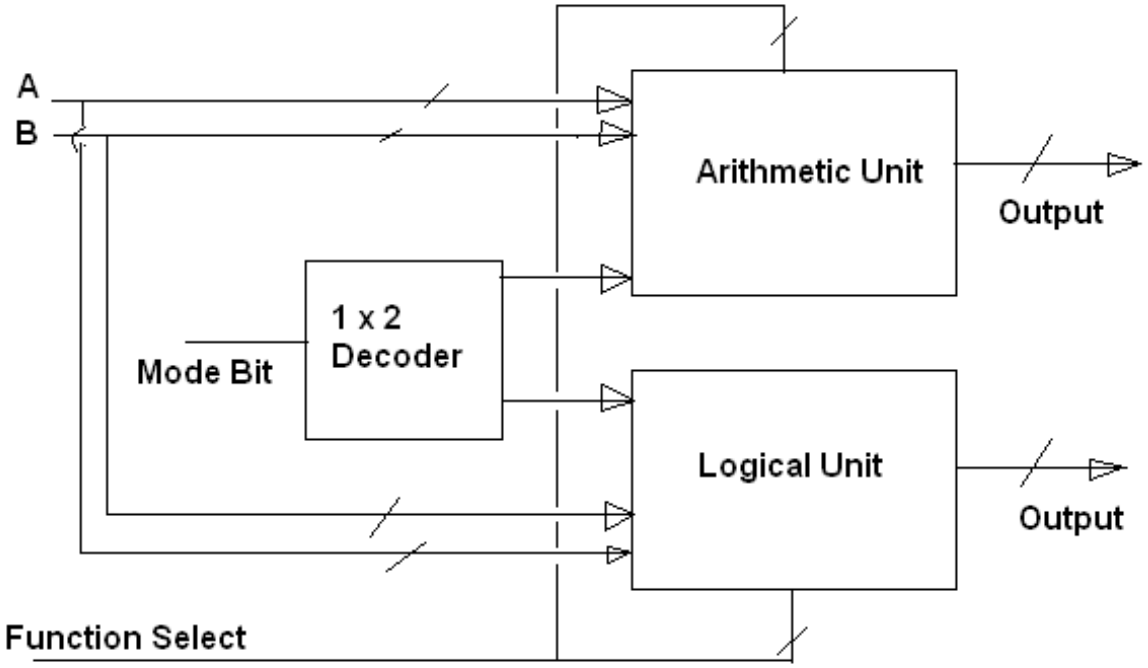


Figure-1: Block Diagram of ALU

The 1x2 selector on the left is as a mode selector to select one of the two units i.e. either the arithmetic unit or the logical unit. The function select lines, and then used to select one of the many functions of arithmetic or the logical type.

MSI package for ALU: - IC 74181 a 4-bit Arithmetic and logical unit:

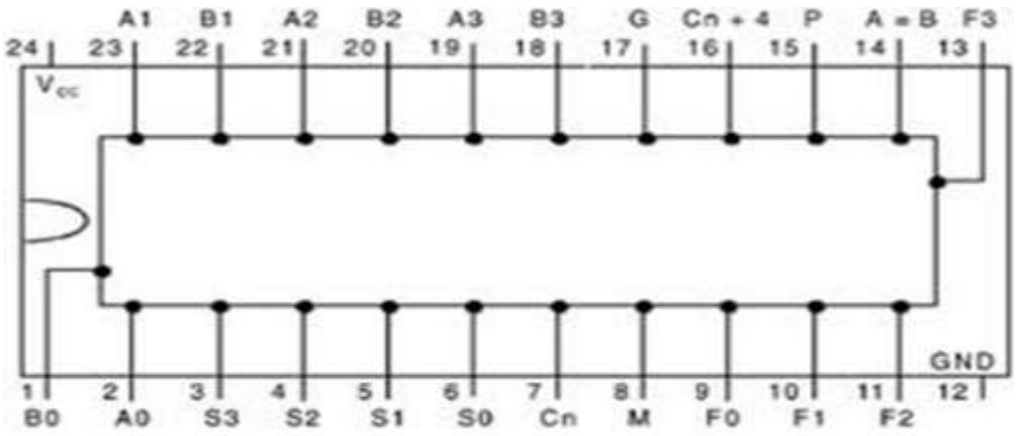


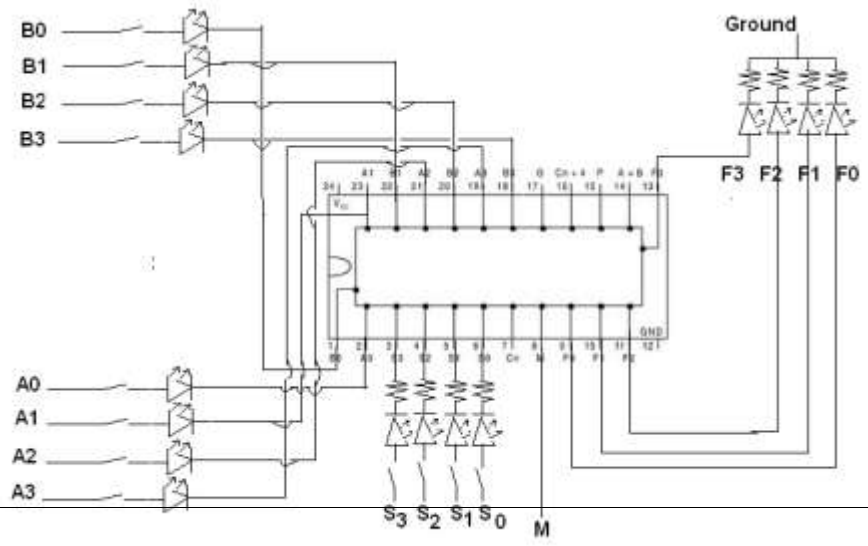
Figure-: Pin Diagram of IC 74181 ALU.

FUNCTION TABLE OF ALU 74181:

S3	S2	S1	S0	$M = 1$	$M = 0$ $CIN = 1$	$M = 0$ $CIN = 0$
0	0	0	0	$\overline{A}$	A	$A + 1$
0	0	0	1	$\overline{A \mid B}$	$A \mid B$	$A \mid B + 1$
0	0	1	0	$\overline{A}B$	$A \mid \overline{B}$	$A \mid \overline{B} + 1$
0	0	1	1	0	-1	0
0	1	0	0	$\overline{AB}$	$A + A\overline{B}$	$A + A\overline{B} + 1$
0	1	0	1	$\overline{B}$	$(A \mid B) + A\overline{B}$	$(A \mid B) + A\overline{B} + 1$
0	1	1	0	$A \oplus B$	$A - B - 1$	$A - B$
0	1	1	1	$A\overline{B}$	$A\overline{B} - 1$	$A\overline{B}$
1	0	0	0	$\overline{A} \mid B$	$A + AB$	$A + AB + 1$
1	0	0	1	$\overline{A \oplus B}$	$A + B$	$A + B + 1$
1	0	1	0	B	$(A \mid \overline{B}) + AB$	$(A \mid \overline{B}) + AB + 1$
1	0	1	1	AB	$AB - 1$	AB
1	1	0	0	1	$2 * A$	$2 * A + 1$
1	1	0	1	$A \mid \overline{B}$	$(A \mid B) + A$	$(A \mid B) + A + 1$
1	1	1	0	$A \mid B$	$(A \mid \overline{B}) + A$	$(A \mid \overline{B}) + A + 1$
1	1	1	1	A	$A - 1$	A

IMPLEMENTATION:

LEDs are connected at the input A and B lines and the select lines to indicate the value of the inputs A and B. The LEDs at the select lines are used to specify the function of the ALU. The LEDs at the output are used to test and verify the output. The whole implementation is shown in figure is



PPRECAUTION:

1. Keep the datasheet of IC 74181 ready.
2. Insert the IC on the Breadboard.
3. Make connections as shown in figure-6
4. Verify the connections

VERIFICATION:

The above circuit when connected to power supply gives correct result as per the function table.